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BRNO UNIVERSITY OF TECHNOLOGY



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UNCONVENTIONAL CIRCUIT ELEMENTS FOR LADDER FILTER DESIGN

DOKTORSKÁ PRÁCE
DOCTORAL THESIS

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BRNO 2011

ABSTRACT

Frequency filters are linear electric circuits that are used in wide area of electronics. They are also the basic building blocks in analogue signal processing.

In the last decade, a huge number of active building blocks for analogue signal processing were introduced. However, there is still the need to develop new active elements that offer new possibilities and better parameters. The current-, voltage-, or mixed-mode analog circuits and their various aspects are discussed in the thesis. This work reflects the trend of low-power (LP) low-voltage (LV) circuits for portable electronic and mobile communication systems and the problems of their design. The need for high-performance LV circuits encourages the analog designers to look for new circuit architectures and new LV techniques.

This thesis presents various active elements such as Operational Transconductance Amplifier (OTA), Current Conveyor of Second Generation (CCII), and Current Differencing Transconductance Amplifier (CDTA), and introduces novel ones, such as Voltage Differencing Transconductance Amplifier (VDTA) and Voltage Differencing Voltage Transconductance Amplifier (VDVTA). All the above active elements were also designed in CMOS bulk-driven technology for LP LV applications.

This thesis is also focused on replacement of conventional inductors by synthetic ones in passive LC ladder filters. These replacements can lead to the synthesis of active filters with interesting parameters.

KEYWORDS

Analog signal processing, current-mode, voltage-mode, frequency filter, first-order all-pass filter, universal filter, KHN, active floating inductance simulator, OTA, CCII, CDTA, DVCC, VDTA, VDVTA.

ANOTACE

Kmitočtové filtry jsou lineární elektrické obvody, které jsou využívány v různých oblastech elektroniky. Současně tvoří základní stavební bloky pro analogové zpracování signálů.

V poslední dekádě bylo zavedeno množství aktivních stavebních bloků pro analogové zpracování signálů. Stále však existuje potřeba vývoje nových aktivních součástek, které by poskytovaly nové možnosti a lepší parametry. V práci jsou diskutovány různé aspekty obvodů pracujících v napěťovém, proudovém a smíšeném módu. Práce reaguje na dnešní potřebu nízkovýkonových aplikací pro přenosné přístroje a mobilní komunikační systémy a na problémy jejich návrhu. Potřeba těchto výkonných nízkonapěťových zařízení je výzvou návrhářů k hledání nových obvodových topologií a nových nízkonapěťových technik.

V práci je popsána řada aktivních prvků, jako například operační transkonduktanční zesilovač (OTA), proudový konvektor II. generace (CCII) a CDTA (Current Differencing Transconductance Amplifier). Dále jsou navrženy nové prvky, jako jsou VDTA (Voltage Differencing Transconductance Amplifier) a VDVTA (Voltage Differencing Voltage Transconductance Amplifier). Všechny tyto prvky byly rovněž implementovány pomocí "bulk-driven" techniky CMOS s cílem realizace nízkonapěťových aplikací.

Tato práce je rovněž zaměřena na náhrady klasických induktorů syntetickými induktory v pasivních LC příčkových filtrech. Tyto náhrady pak mohou vést k syntéze aktivních filtrů se zajímavými vlastnostmi.

KLÍČOVÁ SLOVA

Analogové zpracování signálů, proudový mód, napěťový mód, kmitočtový filtr, fázovací členek 1. řádu, univerzální filtr, KHN, simulátor plovoucího induktoru, OTA, CCII, CDTA, DVCC, VDTA, VDVTA.

SHAKTOUR, M. *Unconventional Circuit Elements for Ladder Filter Design*:doctoral thesis.
Brno: Brno University of Technology, Faculty of Electrical Engineering and Communication,
Department of Microelectronics, 2011. 108 p. Supervised by prof. Ing. Dalibor Biolek, CSc.

DECLARATION

I declare that I have elaborated my doctoral thesis on the theme of “Unconventional Circuit Elements for Ladder Filter Design” independently, under the supervision of the doctoral thesis supervisor and with the use of technical literature and other sources of information which are all quoted in the thesis and detailed in the list of literature at the end of the thesis.

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Brno, 06. 04. 2011.

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(author’s signature)

Acknowledgments

I would like to express my gratitude to my supervisor, Prof. Dalibor Biolek, whose expertise, understanding, and patience, added considerably to my graduate experience.

No teacher in my career has had a larger influence on my development than Prof. Dalibor Biolek. He has always had an open door for questions, comments, or discussions.

My thanks also goes to all those who have provided me with advice and assistance throughout my four years of doctoral study at the Brno University of Technology.

Finally, I thank my family, especially my mother and father, my wife, Zayneb for their support during this process and throughout my life. Everything that I have and will accomplish is a direct reflection of their unending love and encouragement.

LIST OF ABBREVIATIONS

ABB	Active Building Block
AP	All-Pass
BJT	Bipolar Junction Transistor
BOTA	Balanced-Output Operational Transconductance Amplifier
BP	Band-Pass
BS	Band-Stop
CCII	Second-generation Current Conveyor
CCII+/-	Dual-Output Second-generation Current Conveyor
CCs	Current Conveyors
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CDU	Current Differencing Unit
CE	Characteristic Equation
CF	Current Follower
CM	Current Mode
CMOS	Complementary Metal Oxide Semiconductor
DVCC	Differential Voltage Current Conveyor
FDNR	Frequency Dependent Negative Resistor
HP	High-Pass
KHN	Kerwin-Huelsman-Newcomb
LP	Low-Pass
MISO	Multi-Input Single-Output
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational Transconductance Amplifier
SIMO	Single-Input Multi-Output
SITO	Single-Input Three-Outputs
SNAP	Symbolic Network Analysis Program
SPICE	Simulation Program with Integrated Circuit Emphasis
VC	Voltage Conveyor
VDTA	Voltage Differencing Transconductance Amplifier
VDVTA	Voltage Differencing Voltage Transconductance Amplifier
VM	Voltage Mode

LIST OF SYMBOLS

a, b coefficients of general transfer function

a_i coefficients of non-cascade synthesis

C capacitance

D denominator of transfer function

f frequency

f_0 characteristic frequency

ϕ phase of all-pass filter

G conductance

g_m transconductance of the OTA

R resistance

V_{DD}, V_{SS} supply voltages of CMOS structures

W/L CMOS transistor dimensions (Width / Length)

$X, Y, Z+, Z-$ input or output, current or voltage terminals of the CCII

$V_{in+}, V_{in-}, I_{out}$ input or output, current or voltage terminals of the OTA

$p, n, x+, x-$ input or output, current of the CDTA

$V_p, V_n, x+, x-$ input or output, current or voltage terminals of the VDTA

Y admittance

Z impedance

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INTRODUCTION

Filters are widely used in analog signal processing [1] to select the particular frequency. Voltage-mode and current-mode circuits such as current conveyors [2] and current feed back operational amplifiers [3] are getting much attention as compared to other active elements due to wider bandwidth, simple circuitry, low power consumptions and dynamic ranges.

In the last decade, a huge number of active building blocks were introduced for analogue signal processing. However, there is still the need to develop new active elements that offer new and better advantages. This thesis is, therefore, focused on definition of other novel analog building blocks (ABBs) and, furthermore, novel filter structure designs.

In the present days, a number of trends can be noticed in the area of analogue filter and oscillator design, namely reducing the supply voltage of integrated circuits and transition to the current-mode [4]. On the other hand, current-, voltage- and mixed-mode analog circuits design still receives considerable attention of many researches. Therefore, the proposed circuits in this work are working in current-, voltage-, or mixed-mode.

This thesis work discusses the low-voltage analog active elements and their various aspects. The need of high speed, high performance, low power circuits because of the advent of the portable electronic and mobile communication systems and difficulties faced in achieving that in today, this need for high performance LV circuits give encourages the analog designers to look for new circuit architectures, and new LV techniques. Therefore the proposed circuits are implemented using bulk-driven CMOS structures.

The thesis is organized as follows: Chapter 3 presents various active elements. These active building blocks are further used in this thesis for various filters. This Chapter also introduces novel elements defined within this work. As applications, several current, voltage and mixed-mode filter structures utilizing: Operational Transconductance Amplifier (OTA), Current Conveyor of Second Generation (CCII), Current Differencing Transconductance Amplifier (CDTA), Voltage Differencing Transconductance Amplifier (VDTA), and Voltage Differencing Voltage Transconductance Amplifier (VDVTA) are presented in Chapter 4.

Chapter 4 is focused on replacement of conventional inductors by synthetic ones in passive LC ladder filters. It belongs to well-known methods of high-order low-sensitivity filter design. An efficient way of simulating the floating inductor consists in replacing the inductor by these active building blocks. Part of this Chapter focuses on such second-order filter structures that can provide all standard filter responses without changing the circuit topology.

Special attention is paid to Kerwin– Huelsman–Newcomb structure that enables independent control of the quality factor Q and characteristic frequency ω_0 .

To verify the behavior of the proposed circuits, defined active elements are implemented using bulk-driven CMOS structures.

1. State of the art

In the last decade, a huge number of active building blocks (ABBs) were introduced for analogue signal processing.

Due to disadvantages of conventional inductors, active element-based inductor design is very desirable to designers today. During the last few decades, various floating inductors have been created using different high-performance active building blocks. That is why replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design.

The current conveyor (CC) is the basic building block of a number of contemporary applications both in the current and the mixed modes. The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [5]. Two years later, today's widely used second-generation CCII was described in [6], and in 1995 the third-generation CCIII [7]. However, initially, during that time, the current conveyor did not find many applications because its advantages compared to the classical operational amplifier (Op Amp) were not widely appreciated and any IC implementation of Current Conveyors was not available commercially as an off-the-shelf item.

Today, the current conveyor is considered a universal analog building block with wide spread applications in the current-, voltage-, and mixed-mode signal processing. Its features find most applications in the current mode, when its so-called voltage input y is grounded and the current, flowing into the low-impedance input x , is copied by a simple current mirror into the z output.

The demand for a multiple-output current conveyor led to the DO-CCII (Dual-Output CCII), which provides currents I_z of both directions, thus combining both the positive and the negative CCII in a single device [8]. If both currents are of the same polarity, the conveyors are of the CFCCII_p or CFCCII_n types (Current Follower CCII), where the symbol p or n means positive or negative current conveyor [9]. Another generalization is represented by the so-called DVCCII (Differential Voltage Current Conveyor) [10], in which the original "voltage" input y is split into a pair of inputs y_1 and y_2 . The voltage of the x terminal is then given by the voltage difference of the voltage inputs. This offers more freedom during the design of voltage- and mixed-mode applications.

OTA (Operational Transconductance Amplifier) [11] belongs to the most widespread active elements for on-chip implementation of fast frequency filters.

It acts as a voltage-controlled current source with the possibility of electronic adjustment of transconductance g_m .

Recently, the MO-OTA (Multiple Output OTA) has appeared as a generalization of BOTA (Bipolar OTA) and its applications in economical biquadratic filters [12], [13]. However, the drawbacks of such applications are not sufficiently emphasized. Some of them are referred to in [14]: the MO-OTA applications embody relatively high sensitivities to the attainable matching error of the current gains of the current mirrors that form the multiple output of the OTA.

Using the duality principle, the voltage conveyor (VC) has been presented in 1981 [15]. As in the theory of CCs, also here the first- and second-generation VCs (VCI, VCII, IVCI, and IVCII) were described [15], [16], [17], [18]. The best known VC is the plus-type differential current voltage conveyor (DCVC+) [19] that is more often labeled as the current differencing buffered amplifier (CDBA) [20].

By the modification of the CDBA or replacement of the VF (Voltage Follower) by the operational transconductance amplifier (OTA) [21], the current differencing transconductance amplifier (CDTA) [22] has been presented.

The methodology described, which uses the CDU (Current Differencing Unit) or CF (Current Follower) or CI (Current Inverter) as the input unit, and the following simple blocks such as voltage buffer, OTA, and CCII, represents an open system.

Continuing with the variation that the input unit will now implement voltage and not current differences, the Voltage Differencing Transconductance Amplifier (VDTA) has been introduced [23].

Recently, many papers were published about the simulation of passive ladder filters via numerous types of active elements. Direct simulation via inductor replacement by a synthetic element, indirect simulation via Bruton transformation of passive RCL cell and subsequent FDNR implementation, or leap-frog techniques was used.

In such circuits, frequently used active elements are CDBAs [24-26], CAs (Current Amplifiers) [27], MCCCIs (Multi-Output CCCIs) [28], CDTAs [29-31], OTRAs (Operational Transresistance Amplifier) [32], VCCs (Differential Voltage Current Conveyor) [33], CCIs and CFAs [34], [35], DO_OTAs (Differential-Output OTAs) [36], MO_OTAs (Multiple-Output OTAs) [37], and a combination of classical Operational Amplifiers and OTAs [38]. Common drawback of the above circuit topologies consists in the circuit complexity. For example, a floating inductor is modeled via several active devices, and the

resulting filter structure contains large number of components, including floating resistors and capacitors. One exception from this rule is represented by recently introduced building block named CBTA (Current Backward Transconductance Amplifier) which enables simulating n -th order ladder filter via n CBTAs and n grounded capacitors [39], [40].

The above state-of-the-art clearly shows the topicality of the simulation of passive ladder filters via modern active elements as well as searching for such building blocks which would enable economical synthesis of artificial inductors. During the research activities towards finishing this work, it was shown that the VDTA element which was synthesized in the first stage of the research can be a good building block for designing economical ladder simulators.

2. Thesis objectives

The first aim of this thesis is to define various types of novel active building blocks for the effective synthesis of filter simulating RLC ladder structure. The second aim is to perform such a synthesis.

The first part of the thesis focuses on designing a high linearity, wideband bulk-driven OTA with tunable transconductance. This OTA is then used for designing active building blocks (CDTA, VDTA, VDVTA, and DVCC). As applications, several filters structures current-, voltage- and mixed-mode by using VDTA are presented, particularly the second-order filter structures that can provide all standard filter responses without changing the circuit topology. Special attention is paid to Kerwin–Huelsman–Newcomb structure that enables independent control of the quality factor Q and characteristic frequency ω_0 .

The second part of thesis deals with LC ladder simulation on the principle of inductor replacement by synthetic inductor.

The floating inductor is synthesized via:

1. MAX435, a commercial OTA [57], [64], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well-known circuitry for simulating the floating inductor. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.
2. „super-transistor“ (S-T), which is commercially available in several versions, e.g. OPA615, SHC615, OPA860, and OPA861 [64].
3. Newly introduced VDTA and VDVTA elements [55] designed in the first part of the thesis.

All the designs are verified in two steps:

In the first step, the theoretical analyses are done using SNAP software [41]. To verify the complex behavior of the proposed circuits, SPICE simulations are performed, utilizing transistor-level models of active elements.

3. Active building blocks and their properties

The following active elements are devices having multi ports with properties that make them useful in network synthesis [50]. Some active elements are more useful than others, depending of various design requirements.

3.1. Operational Transconductance Amplifier (OTA)

The OTAs were made commercially available for the first time in 1969 by RCA. The first publications with OTA came out in 1985, when authors in [21] presented to the general public the new CMOS OTA architectures and new filter realizations.

An ideal operational transconductance amplifier is a voltage-controlled current source, with infinite input and output impedances and frequency independent transconductance. OTA has two attractive features: 1) changing the external dc bias current or voltage can control its transconductance, and 2) It can work at high frequencies.

This research thesis focuses on the MOS implementations of the transconductance amplifiers. OTA is a voltage controlled current source.

More specifically, the term “operational” comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal OTA is a differential-input voltage-controlled current source (DVCCS). Its symbol is shown in Fig. 3-1 (a), and its operation is defined by the following equation (3-1). Both voltages V_+ and V_- are with reference to ground. The equivalent circuit of the ideal OTA is shown in Fig. 3-1 (b).

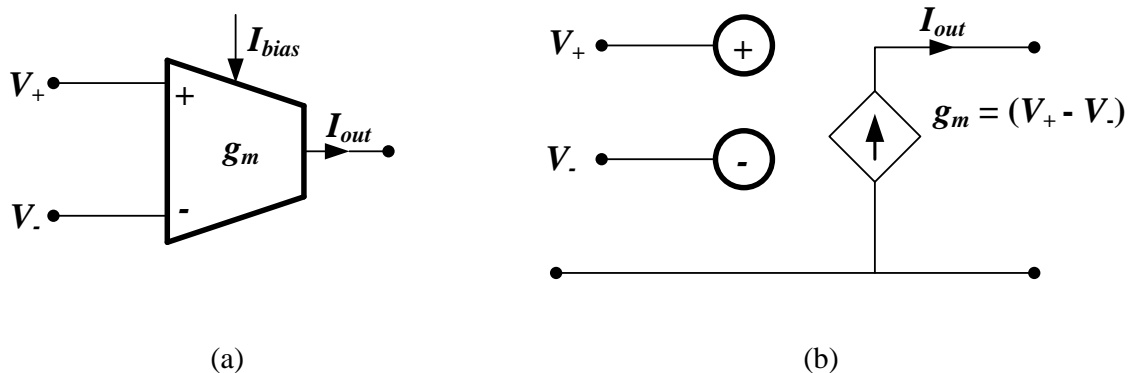


Fig. 3-1: (a) OTA symbol, (b) ideal equivalent circuit.

$$I_{out} = g_m(V_+ - V_-) \quad (3-1)$$

Currently, the OTA elements are supplied on the market by many manufacturers [53].

A commercially available OTA elements are, for example, LT1228 (Linear Technology) or MAX435 (MAXIM-Dallas Semiconductor). The latter is a high-speed wideband transconductance amplifier (WTA) with high-impedance inputs and output. Due to its unique performance features, it is suitable for a wide variety of applications such as high-speed instrumentation amplifiers, wideband, high-speed RF filters, and high-speed differential line driver and receiver applications.

3.1.1. Operations using ideal OTA

- **Voltage Amplification using OTA**

Inverting and noninverting voltage amplification can be achieved using an OTA as shown in Fig. 3-2 (a) and 3-2 (b), respectively [50]. Any desired gain can be achieved by a proper choice of g_m and R_L . It should be noted that the output voltage V_o is obtained from a source with output impedance equal to R_L . Zero output impedance can be achieved only if such circuits are followed by a voltage follower.

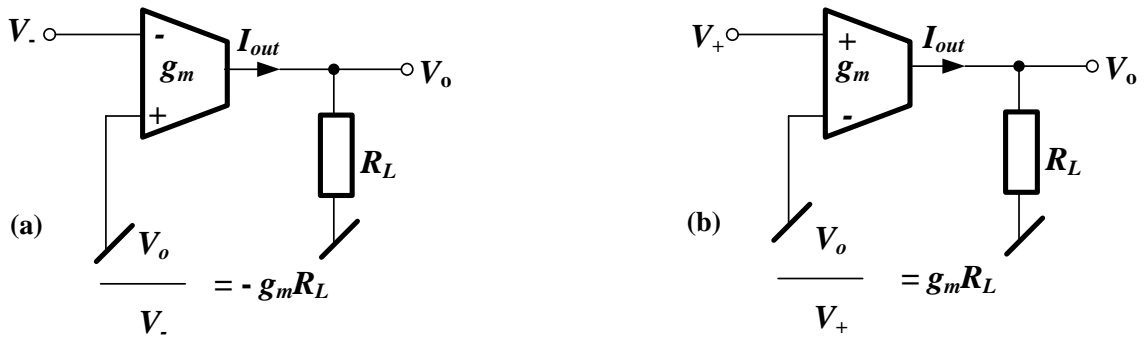


Fig. 3-2: (a) Inverting and (b) noninverting voltage amplifier using OTA.

- **A Voltage –Variable Resistor (VVR)**

A grounded voltage-variable resistor can be easily obtained using an ideal OTA as shown in Fig. 3-3. Since $I_{out} = -I_{in}$, we have the following [50]:

$$Z_{in} = \frac{V_-}{I_{in}} = \frac{V_-}{-I_{out}} = \frac{V_-}{g_m V_-} = \frac{1}{g_m} \quad (3-2)$$

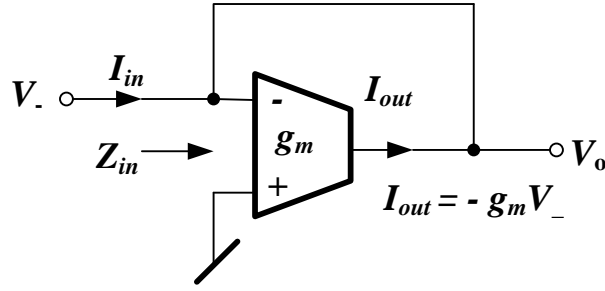


Fig. 3-3: Grounded voltage-variable resistor using OTA.

Using two such arrangements cross-connected in parallel, a floating VVR can be obtained. On the other hand, if the input terminals in Fig. 3-3 are interchanged, the input resistance will be $-1/g_m$. Thus, using OTAs, both positive and negative resistors become available without actually having to build them on the chip. These, coupled with capacitors, lead to the creation of the so called active- C filters.

- **Voltage summation using OTA**

Voltage summation can be obtained using OTAs, which in effect translate voltages to currents. Currents are easily summed as shown in Fig. 3-4.

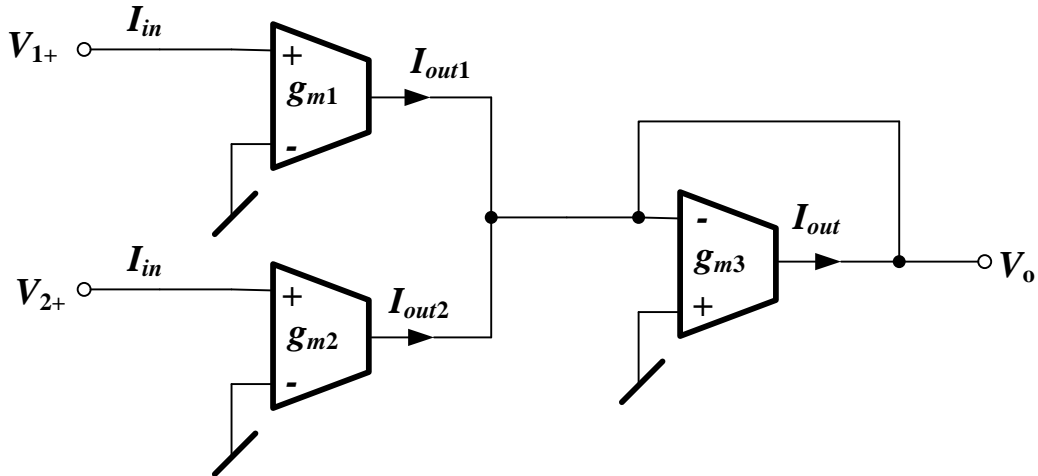


Fig. 3-4: Voltage summation using OTA.

It is clear that

$$I_{out1} + I_{out2} + I_{out} = 0 \quad (3-3)$$

$$g_{m1}V_{1+} + g_{m2}V_{2+} - g_{m3}V_o = 0 \quad (3-4)$$

$$V_o = \frac{g_{m1}}{g_{m3}} V_{1+} + \frac{g_{m2}}{g_{m3}} V_{2+} \quad (3-5)$$

If $g_{m1} = g_{m2} = g_{m3}$

$$V_o = V_{1+} + V_{2+} \quad (3-6)$$

By changing the grounded input of one of the input OTAs, voltage subtraction can be achieved. These operations are useful for the realization of filters which should be synthesized from their transfer functions.

- **Integrator using OTA**

The operation of integration can be achieved very conveniently using the OTA as is shown in Fig. 3-5. The following equations can be written for Fig. 3-5 a) and b), respectively:

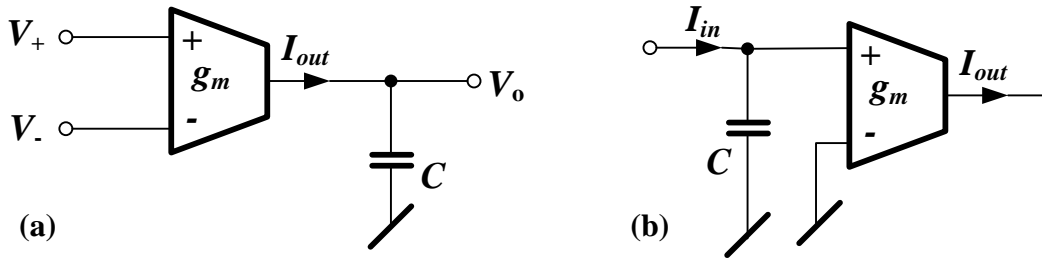


Fig. 3-5: Integrators using OTA, (a) voltage-mode, (b) current-mode.

$$V_o = \frac{I_{out}}{sC} = \frac{g_m}{sC} (V_+ - V_-) \quad (3-7)$$

$$I_{out} = \frac{g_m}{sC} I_{in}$$

3.1.2. CMOS Implementation of OTA

Bulk-driven CMOS implementation of OTA shown in Fig. 3-6 consists of two stage, the first which combined of the bulk-driven differential stage with pMOS input device M_1 and M_2 and the current mirror M_3 and M_4 acting as an active load [54]. The second stage is a simple CMOS inverter with M_6 as a driver and M_7 acting as an active load. Its output is connected to the output of the differential stage by means of compensation capacitance C_c and the resistance R_C since the compensation capacitance actually acts as a Miller capacitance in the

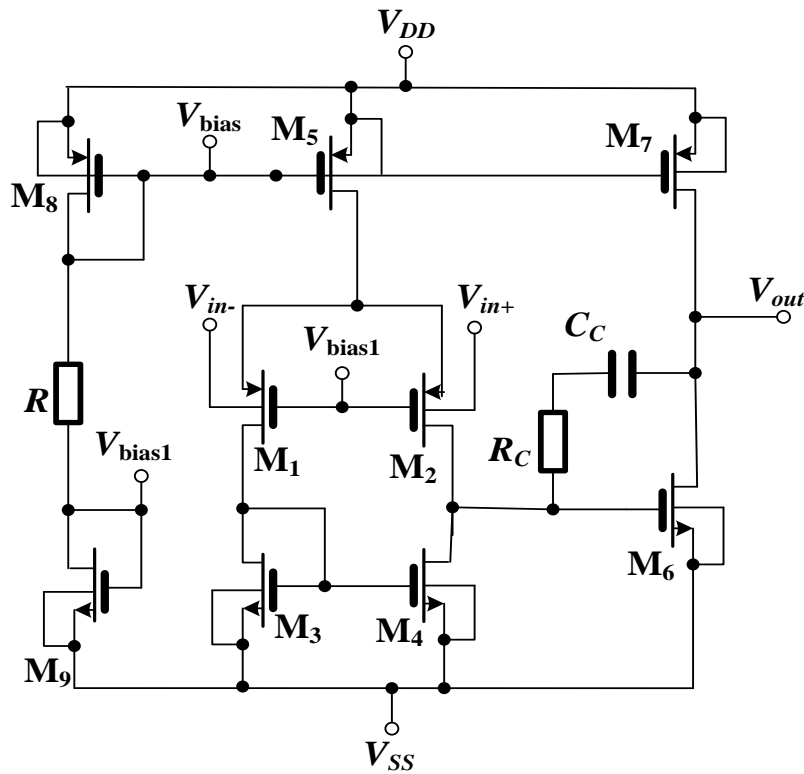


Fig. 3-6: Two stages Bulk-driven OTA [54].

Characteristics	Simulation Result
Power consumption	30 μ W
Open loop gain	70 dB
Bandwidth	4 MHz
Phase margin	70°
DC input voltage range	-400, 700mV
Slow rate	SR _{LH} = 0.8V/ μ s , SR _{HL} = 0.4V/ μ s
Measurement condition: V _{DD} = 0.6V, V _{SS} = 0.6V, C _L = 1pF	

Tab. 3.1: Simulation results of the Bulk-driven OTA.

3.2. Current Conveyor of Second Generation (CCII)

One of the most basic building blocks in the area of current-mode analogue signal processing is the current conveyor (CC). The principle of the current conveyor of the first generation was published in 1968 by K. C. Smith and A. S. Sedra [5]. CCI was then replaced by a more versatile second-generation device in 1970 [6], the CCII. Current conveyor designs

have mainly been with BJTs due to their high transconductance values compared to their CMOS counterparts. They are used as current-feedback operational amplifiers like the MAX477 high-speed amplifier and the MAX4112 low-power amplifier, which both feature current feedback rather than the conventional voltage feedback used by standard operational amplifiers.

Current conveyors are used in high-frequency applications where the conventional operational amplifiers can not be used, because the conventional designs are limited by their gain-bandwidth product.

The second-generation current conveyor (CCII) is used as a basic building block in many current-mode analog circuits. It is a three-terminal (X, Y and Z) device as shown in Fig. 3-7 (a), and the equivalent circuit of the ideal CCII is shown in Fig. 3-7 (b).

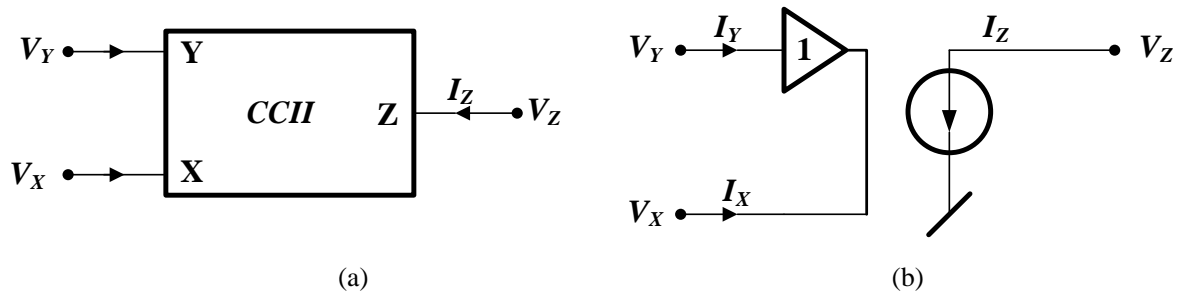


Fig. 3-7: (a) The CCII symbol, (b) ideal equivalent circuit.

The characteristics of ideal CCII are represented by the following hybrid matrix

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (3-8)$$

An ideal CCII has the following characteristics:

- Infinite input impedance at terminal Y ($R_Y = \infty$ and $I_Y = 0$)
- Zero input impedance at terminal X ($R_X = 0$)
- Accurate voltage copy from terminal Y to X ($V_X = V_Y$)
- Accurate current copy from terminal X to Z with infinite output impedance at Z ($I_Z = I_X$ and $R_Z = \infty$)

3.2.1. Operations using the ideal CCII

- **Amplifiers using CCII**

The CCII can easily be used to form the current output amplifiers and voltage-output amplifier as shown in Fig. 3-8. The voltage- and current- gains are as follows:

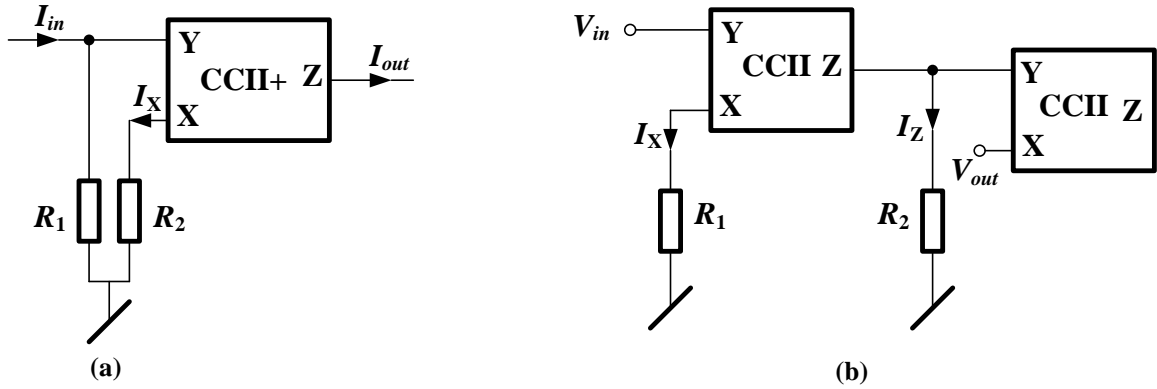


Fig. 3-8: (a) CCII-based current amplifier, (b) CCII-based voltage amplifier.

$$\frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} \quad (3-9)$$

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} \quad (3-10)$$

- **Integrators using CCII**

In Fig. 3-9, simple current- and voltage- integrators are presented.

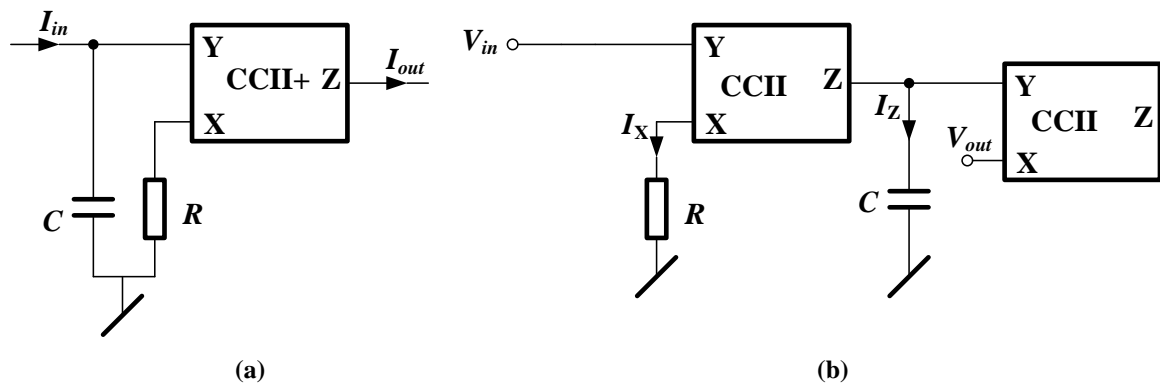


Fig. 3-9: (a) CCII-based current integrator, (b) CCII-based voltage integrator.

The output signals are as follows:

$$I_{out} = \frac{I_{in}}{sCR} \quad (3-11)$$

$$V_{out} = \frac{V_{in}}{sCR} \quad (3-12)$$

- **Adders using CCII**

In Fig. 3-10, CCII-based current adder and CCII-based voltage adder are reported, with the following equations:

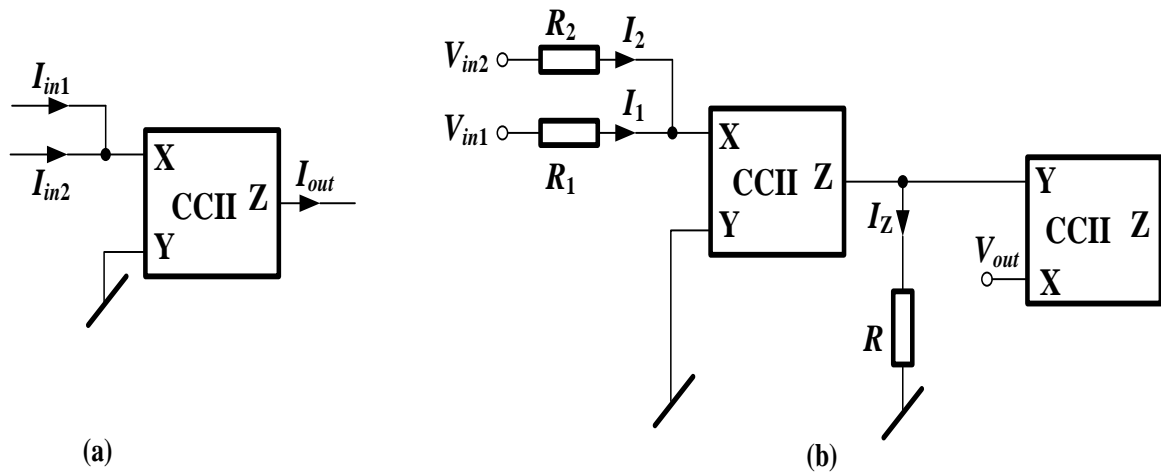


Fig. 3-10: (a) CCII-based current adder, (b) CCII-based voltage adder.

$$I_{out} = -(I_{in1} + I_{in2}) \quad (3-13)$$

$$V_{out} = -\frac{R}{R_1} V_{in1} - \frac{R}{R_2} V_{in2} \quad (3-14)$$

- **Differentiators using CCII**

Current- and voltage-mode versions are shown in Fig. 3-11. The output signals are as follows:

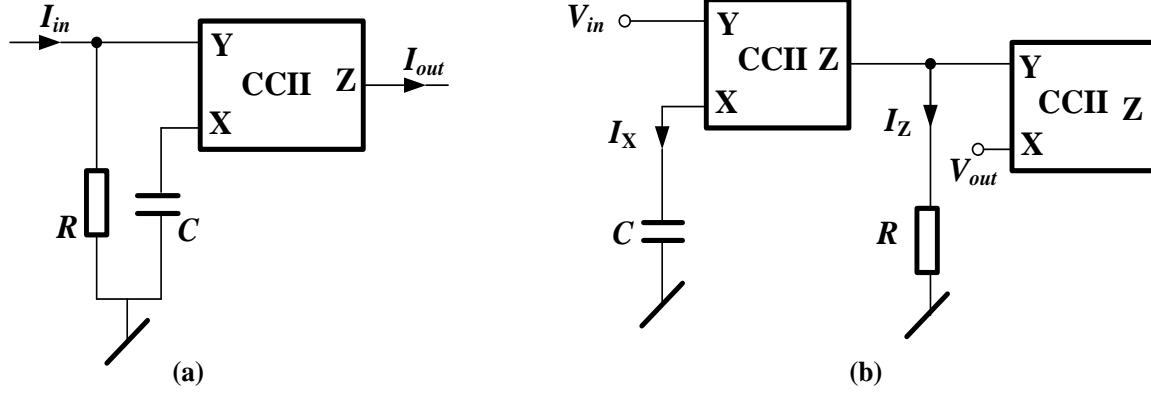


Fig. 3-11: (a) CCII-based current differentiator, (b) CCII-based voltage differentiator.

$$I_{out} = sCR I_{in} \quad (3-15)$$

$$V_{out} = sCR V_{in} \quad (3-16)$$

3.2.2. Bulk-driven CCII± based on Bulk-driven OTA

A new connection of Bulk-driven OTA is used to realize the CCII. In the OTA-based approach, presented in Fig.3-12, Bulk-driven OTA is used to implement the unity gain buffer between the Y and X inputs [54]. The X input current I_X is sensed by duplicating buffers' output transistors M_6 and M_7 using transistors M_8 and M_9 , and extracting the X current from them as I_Z . Since transistors M_8 and M_9 have the same size and gate-source voltage as the output stage transistors M_6 and M_7 , the current I_Z should be a copy of the current flowing through M_6 and M_7 which is I_X . Transistors M_{10} - M_{15} are used to generate I_Z . Since no additional transistors need to be inserted between the OTA and rails, the approach will not increase the minimum operating voltage over that of the operational core. In addition the voltage follower is based on an OTA, thus it will maintain all the benefits and also the disadvantages of such a circuit i.e. a good voltage follower at the cost of lower bandwidth.

The simulated frequency responses of current gains I_{z+}/I_x , I_{z-}/I_x are given in Fig. 3-13. The cutoff frequencies for the gains are 20 MHz and 52 MHz, respectively.

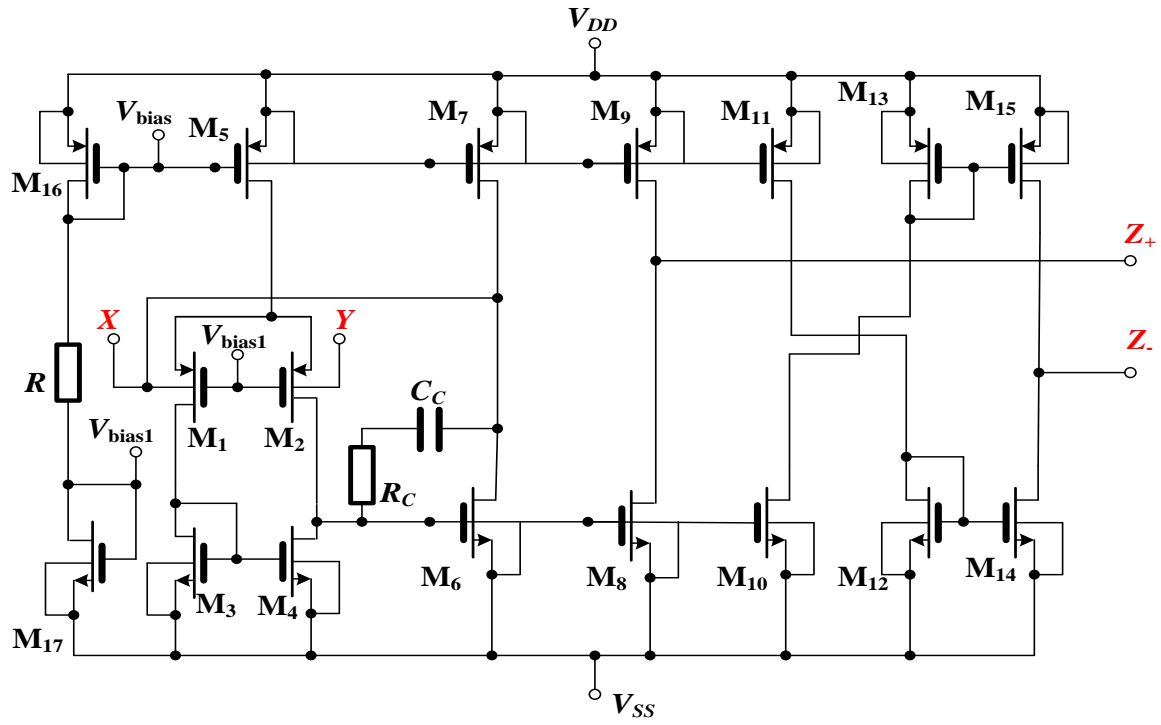


Fig. 3-12: Bulk-driven CCII± based on Bulk-driven OTA.

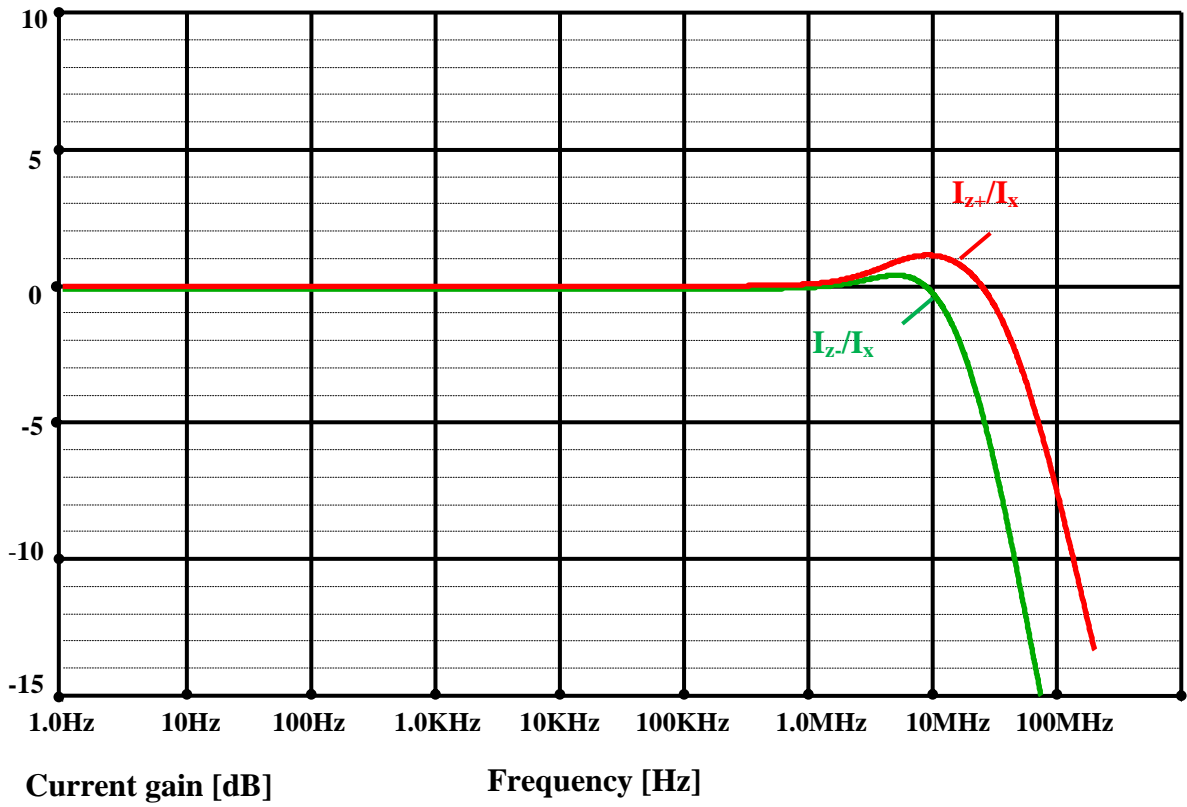


Fig. 3-13: Frequency variation of the current gains I_{Z+}/I_X , I_{Z-}/I_X in Db of the CCII in Fig. 3-12.

In Fig. 3-14, the input voltage buffer behavior is shown. A DC sweep simulation has been performed, to check the range in which the voltage on X node is equal to the voltage applied to Y node.

The current linearity between X and Y terminal of the bulk-driven current conveyor (CCII \pm) from Fig. 3-12, is demonstrated in Fig. 3-15. Note that for input currents I_x and I_z , the boundary of linear operation is ca $\pm 16\mu\text{A}$.

The corresponding small-signal current gains are as follows: I_{z+}/I_X , $I_{z-}/I_X = 1$, and the corresponding voltage gain $V_X/V_Y = 0.97$.

The small-signal low frequency resistance of the X terminal R_x is equal to $166\ \Omega$ as shown in Fig. 3-16. The small-signal resistance of the Y terminal R_Y is equal to $50\text{G}\Omega$. The small-low frequency signal resistances of the Z+, Z- outputs terminals are equal to $560\text{k}\Omega$, and $554\text{k}\Omega$, respectively. Simulation results of the CCII \pm are summarized in Table 3-2.

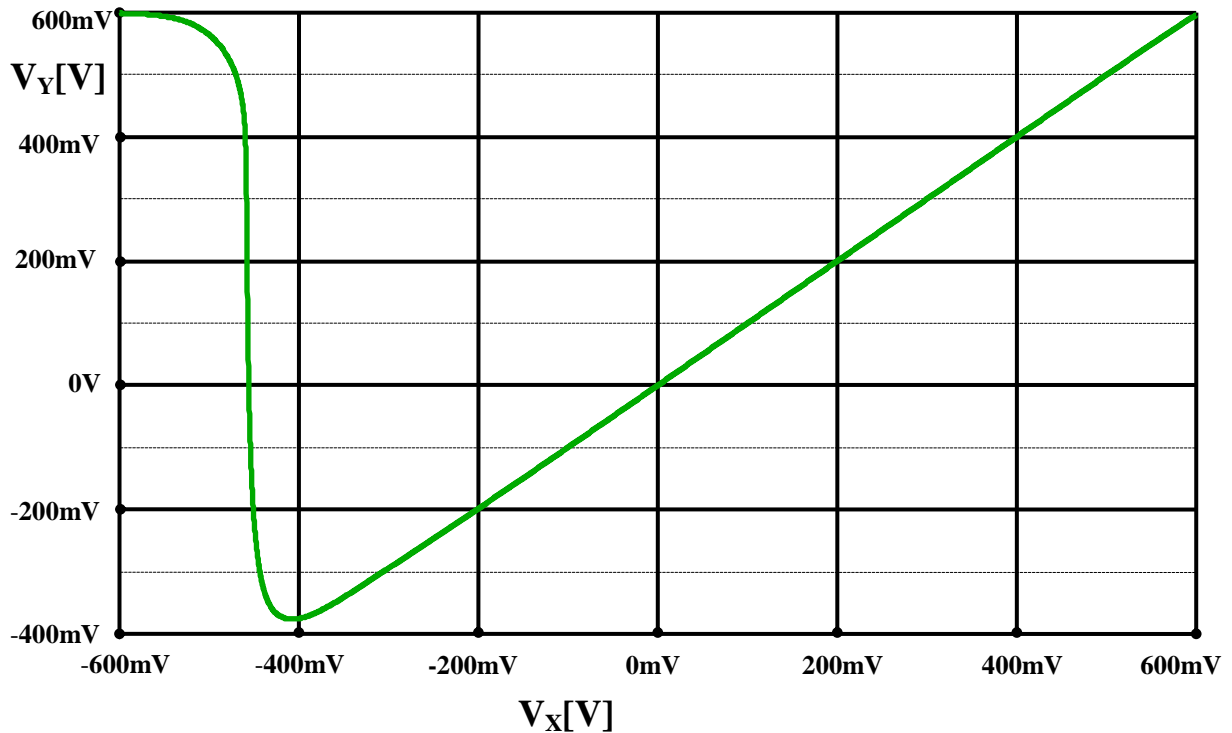


Fig. 3-14: Voltage follower between X and Y of the CCII in Fig. 3-12.

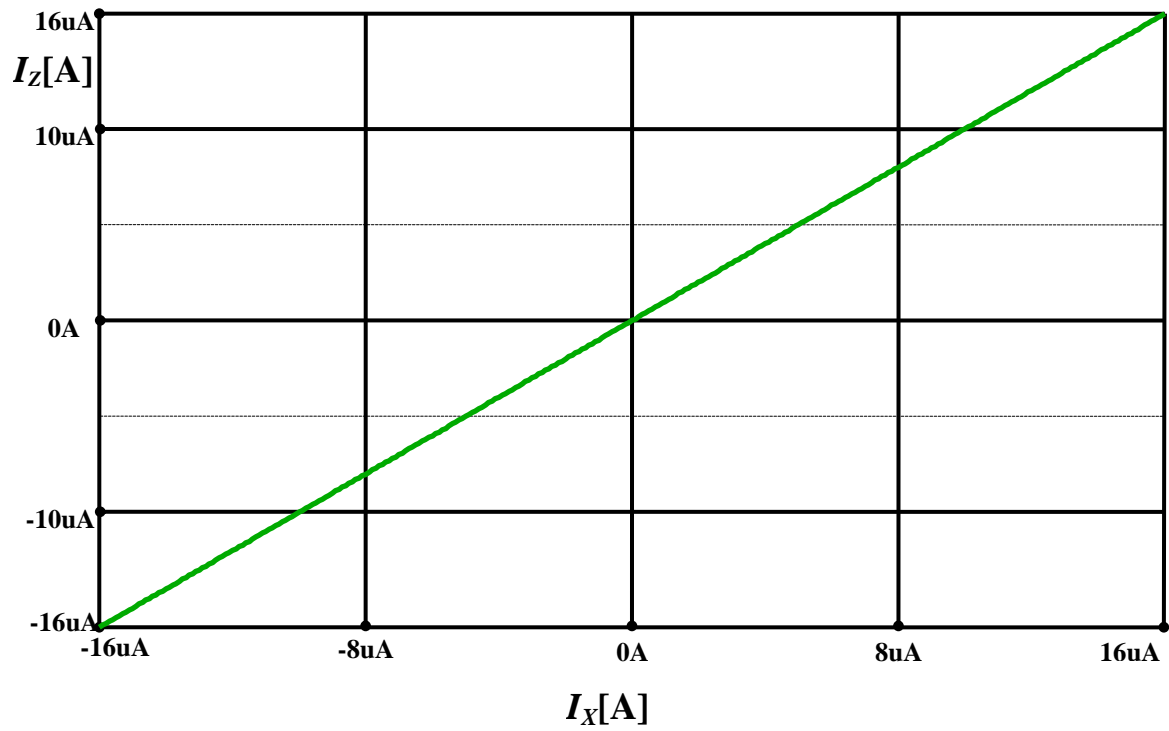


Fig. 3-15: Current linearity between X and Y of the CCII in Fig. 3-12.

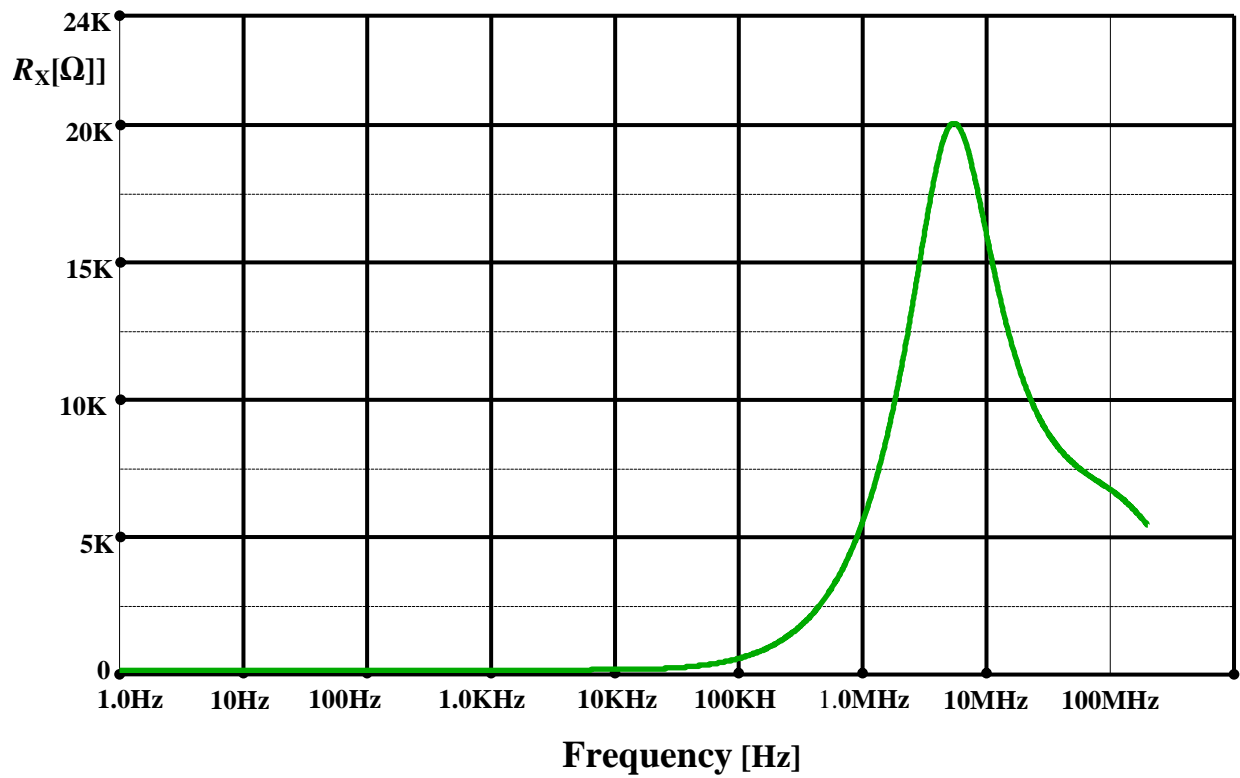


Fig. 3-16: The X node input resistance $r_{in,x}$ of the CCII in Fig. 3-12.

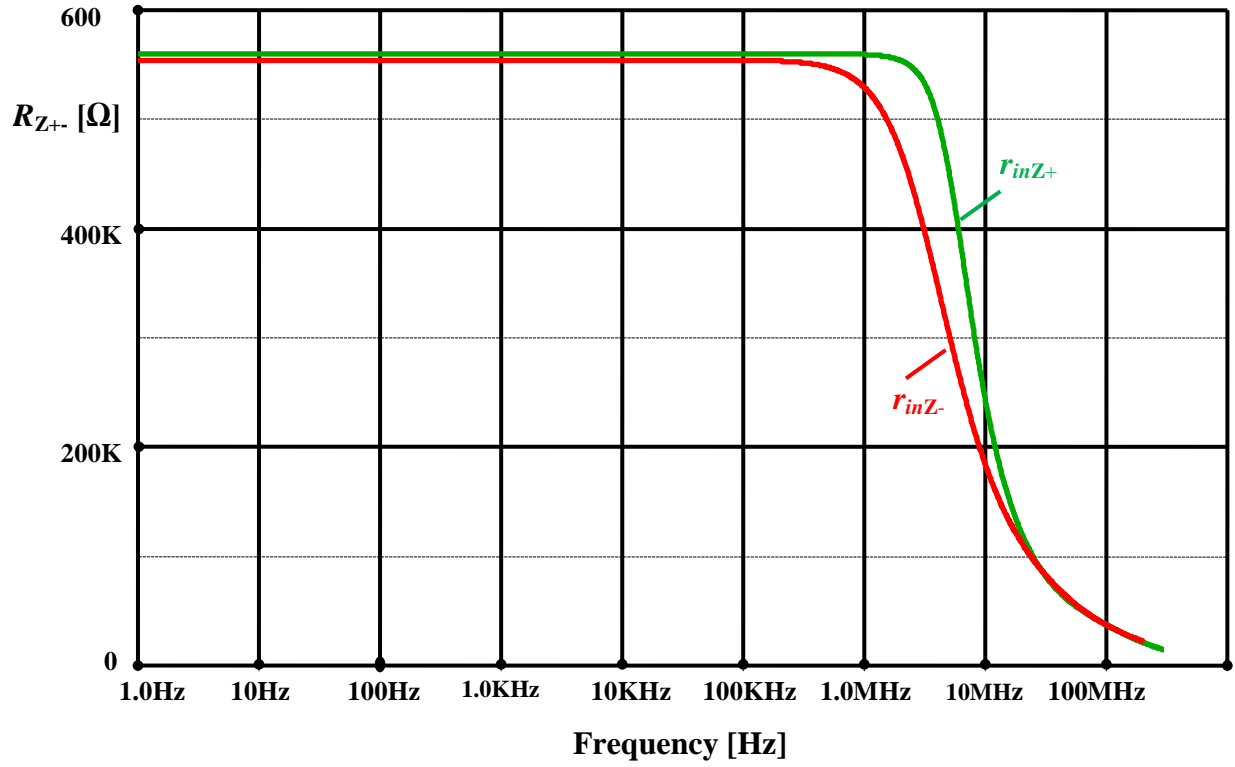


Fig. 3-17: The Z node output resistance $r_{in,Z}$ of the CCII in Fig. 3-12.

Characteristics	Simulation Result
Power consumption	119 μ W
3-dB bandwidth I_{Z+}/I_X	20 MHz
3-dB bandwidth I_Z/I_X	52 MHz
DC voltage range	-400, 600 mV
DC current range	$\pm 16 \mu$ A
Current gain I_Z/I_X	1
Voltage gain V_X/V_Y	0.97
Node X parasitic DC resistance	166 Ω
Node Y parasitic DC resistance	50 G Ω
Node Z+ parasitic DC resistance	560 k Ω
Node Z- parasitic DC resistance	554 k Ω
Measurement condition: $V_{DD} = 0.6V$, $V_{SS} = -0.6V$	

Tab. 3-2: Simulation results of the Bulk-driven CCII.

3.2.3. Bulk-driven OTA with g_m adjustable via external R

In this part, a new concept of high-linearity OTA with controllable transconductance is proposed. The OTA is simulated in a standard TSMC 0.18 μm CMOS process with a 0.6 V supply voltage.

The principle of g_m adjustable via a feedback resistor R_{adj} is show in Fig. 3-18.

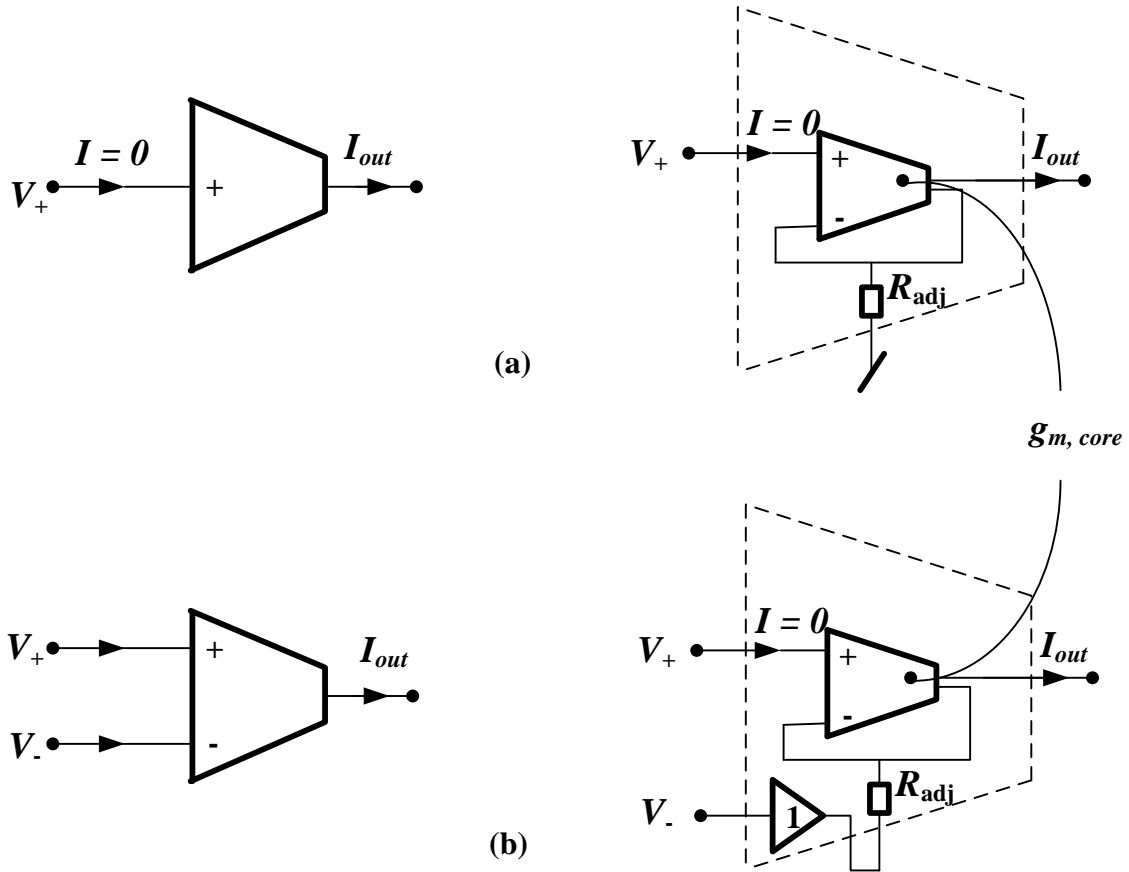


Fig. 3-18: (a) SISO OTA with g_m adjustable, (b) DISO OTA with g_m adjustable.

In this part, a high linearity, wideband OTA with tunable transconductance is presented according to Eq. (3-18). The adjustable transconductance $g_{m,adjust}$ depends on R_{adj} as follows:

$$g_{m,adjust} = \frac{g_{m,core}}{1 + g_{m,core} R_{adj}} \quad (3-17)$$

Figs. 3-19, and 3-20 show circuit implementations of Fig.3.18, namely bulk-driven single input single output OTA (SISO) and a fully differential OTA (DIDO) based on voltage buffer and Current Conveyor of Second Generation CCII.

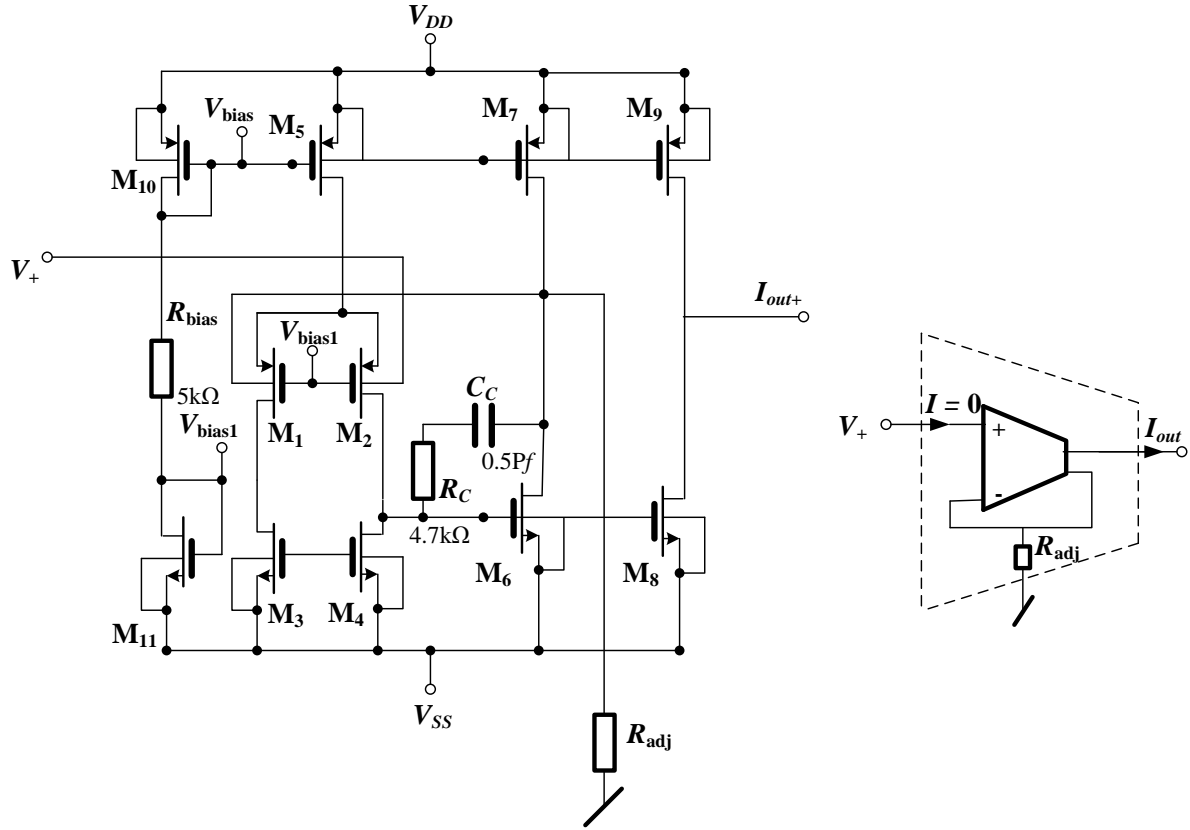


Fig. 3-19: Bulk-driven single input single output OTA (SISO) based on CCII.

The aspect ratios of each of the transistors used the CCII and voltage buffer in Fig. 3-20 are listed in Tables 3-3 and 3-4, respectively.

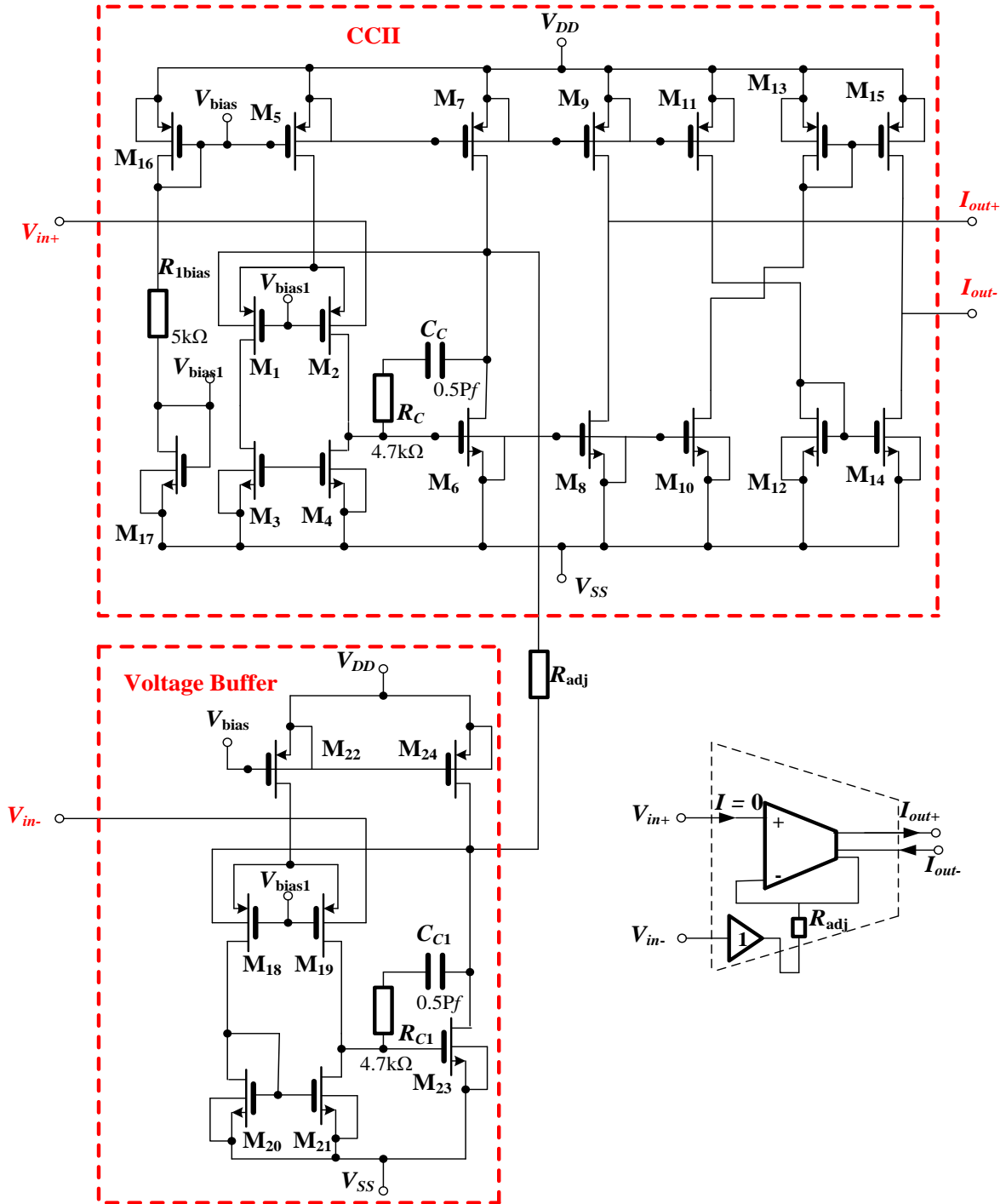


Fig. 3-20: Bulk-driven fully differential OTA (DIDO) based on CCII and voltage buffer.

Transistor	Length (μm)	Width (μm)
M_1, M_2	2	30
M_3, M_4	2	4
M_5, M_{16}	3	20
$M_6, M_8, M_{10}, M_{12}, M_{14}$	2	16
$M_7, M_9, M_{11}, M_{13}, M_{15}$	3	40
M_{17}	3	10

Tab. 3-3: Aspect ratios of the transistors used in the CCII in Fig. 3-20.

Transistor	Length (μm)	Width (μm)
M_{18}, M_{19}	2	30
M_{20}, M_{21}	2	4
M_{22}	3	20
M_{23}	2	16
M_{24}	3	40

Tab: 3-4: Aspect ratios of the transistors used in the Voltage buffer in Fig. 3-20.

The performance of the proposed OTA in Fig. 3-20 was verified via PSPICE simulation. All the balanced CMOS OTA was simulated by using CMOS structure and MIETEC 0.18 μm . The dimensions of transistors were used from Tables. 3-3 and 3-4 and the power supply voltages were set $V_{DD} = -V_{SS} = \pm 0.6\text{V}$.

Fig. 3-21 shows the simulated transfer characteristics of the OTA in Fig. 3-20. The plots of the output current I_{out} versus the input voltage V_{in} show that, for R_{adj} values of 1 Ω , 10 Ω , 100 Ω , 1k Ω , 2k Ω , 5k Ω , 10k Ω , 20k Ω , 50k Ω , 100k Ω , 200k Ω , 500k Ω , and 1M Ω , the g_m is controlled accordingly.

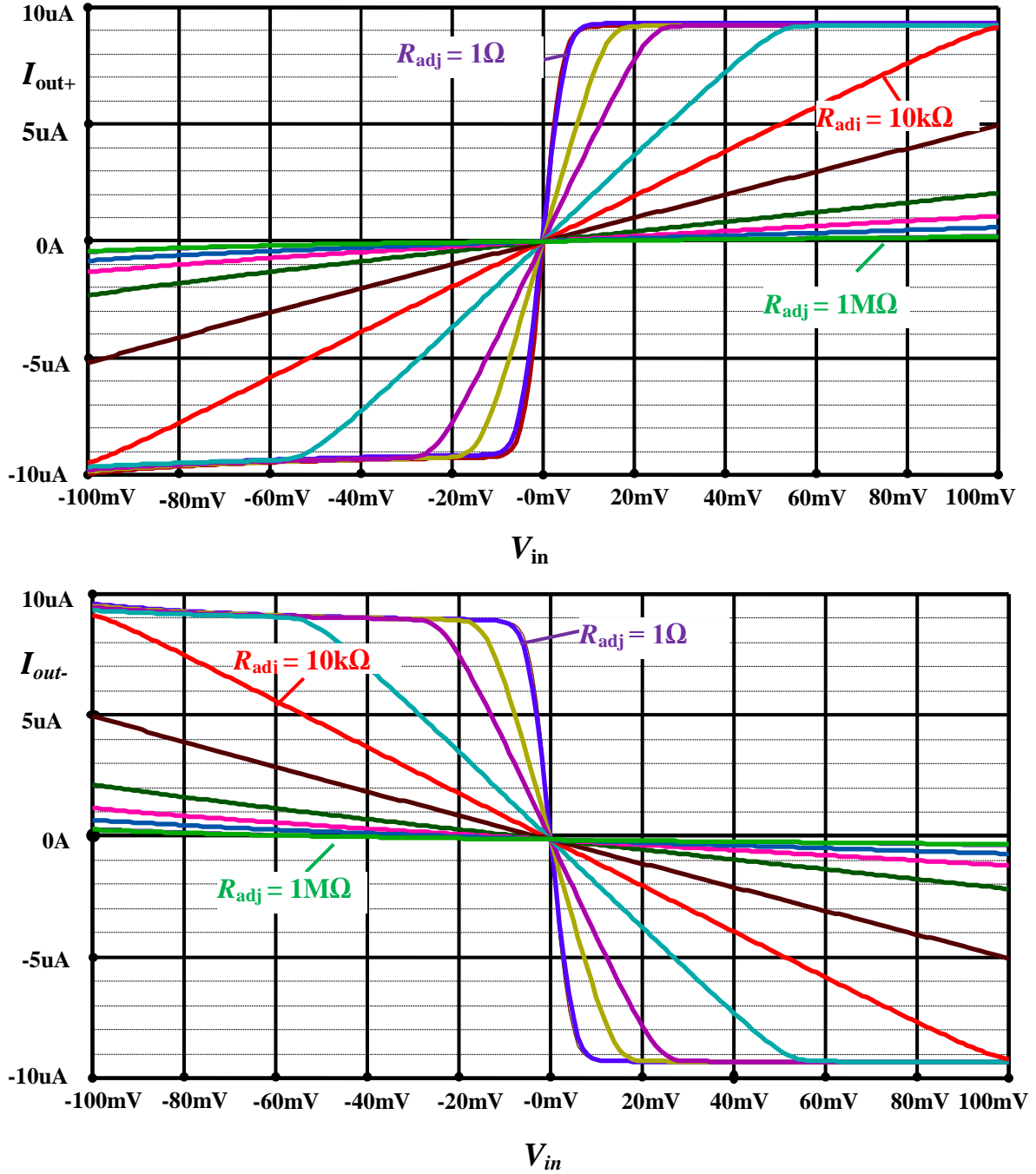


Fig. 3-21: DC transfer characteristics of bulk-driven fully differential OTA.

It is shown that the transconductance gain g_m can be linearly tuned when R_{adj} is increased. But for R_{adj} bigger than 50k Ω it causes distortion. The linear range is very good for R_{adj} of about 10k Ω .

The AC analysis of the bulk-driven OTA in Fig. 3.20 is shown in Fig. 3-22. The frequency dependence of I_{out} is measured by fixing AC value of V_{in} at 1V.

The responses are plotted for R_{adj} of 1 Ω , 10 Ω , 100 Ω , 1k Ω , 2k Ω , 5k Ω , 10k Ω , 20k Ω , 50k Ω , 100k Ω , 200k Ω , 500k Ω , and 1M Ω . The corresponding values of g_m are shown in Table. 3-5

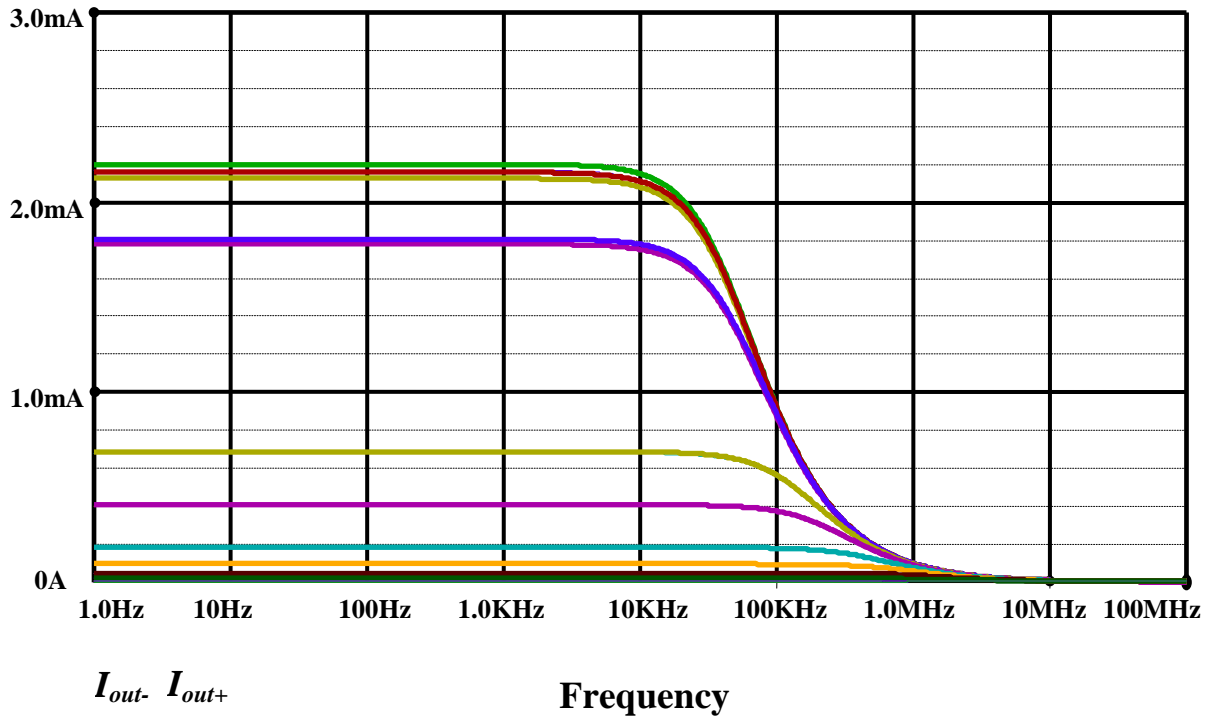


Fig. 3-22: AC transfer characteristics of bulk-driven fully differential OTA.

R_{adj}	g_m
1Ω	2.2 ms
10Ω	2.16 ms
100Ω	1.8 ms
1kΩ	688.7 μs
2kΩ	408.5 μs
50 kΩ	184.45 μs
100 kΩ	96.82 μs
200 kΩ	50.1 μs
500 kΩ	21.04 μs
1 MΩ	11.2 μs

Tab: 3-5: Variations of g_m by R_{adj} .

3.3. Current Differencing Transconductance Amplifier (CDTA)

The CDTA element [55] with its schematic symbol in Fig. 3-23 (a) has a pair of low-impedance current inputs p and n, and an auxiliary terminal z, whose outgoing current is the difference of input currents. Also in Fig. 3-23 (b) is given a possible implementation of

CDTA using the OTA components. Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance g_m and the voltage at the z terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

$$V_p = V_n = 0, \quad I_z = I_p - I_n \quad (3-18)$$

$$I_{x+} = g_m V_z, \quad I_{x-} = -g_m V_z \quad (3-19)$$

Where $V_z = I_z Z_z$ and Z_z is the external impedance connected to z terminal of the CDTA. CDTA can be thought as a combination of a current differencing unit [13] followed by a dual-output operational transconductance amplifier, DO-OTA. Ideally, the OTA is assumed as an ideal voltage-controlled current source and can be described by $I_x = g_m(V_+ - V_-)$, where I_x is output current, V_+ and V_- denote non-inverting and inverting input voltage of the OTA, respectively.

CDTA applications do not require the use of external resistors, which are substituted by internal transconductors. Analogously to the well-known “ $g_m C$ ” applications, the “CDTA-C” circuits are formed by CDTA elements and grounded capacitors. Such structures are well-suited for on-chip implementation.

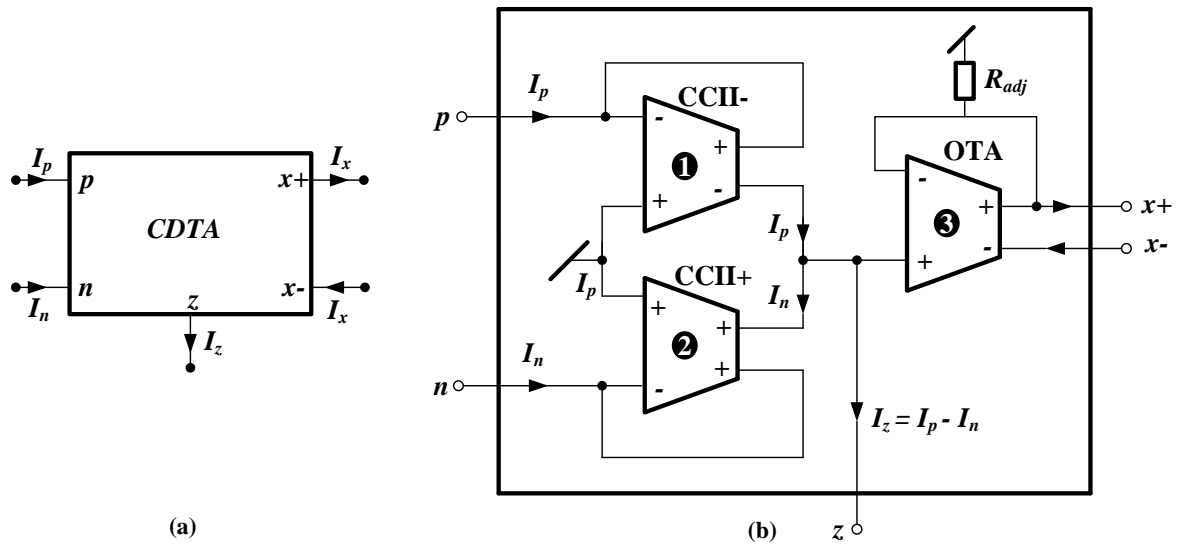


Fig. 3-23: (a) Symbol of the CDTA, (b) its implementation by bulk-driven OTAs.

Marking the voltages of p , n , x , and z terminals in Fig. 3-23 (a) with symbols V_p , V_n , V_x , and V_z , then for the CDTA+- element the following equations are true:

$$\begin{pmatrix} I_z \\ I_{x+} \\ I_{x-} \\ V_p \\ V_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 & -1 \\ g_m & 0 & 0 & 0 & 0 \\ -g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_z \\ V_{x+} \\ V_{x-} \\ I_p \\ I_n \end{pmatrix} \quad (3-20)$$

3.3.1. Operations using the ideal CDTA

- **Integrator using CDTA**

The operation of integration can be achieved very conveniently using the CDTA as shown in Fig. 3-24. Clearly [56],

$$K_i = \frac{I_x}{I_p} = \frac{g_m}{sC} \quad (3-21)$$

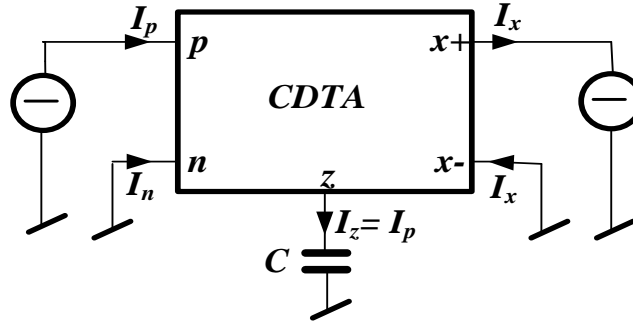


Fig. 3-24: Integrator using CDTA.

- **Current Summation using CDTA**

Current summation can be obtained using CDTA as shown in Fig. 3-25.

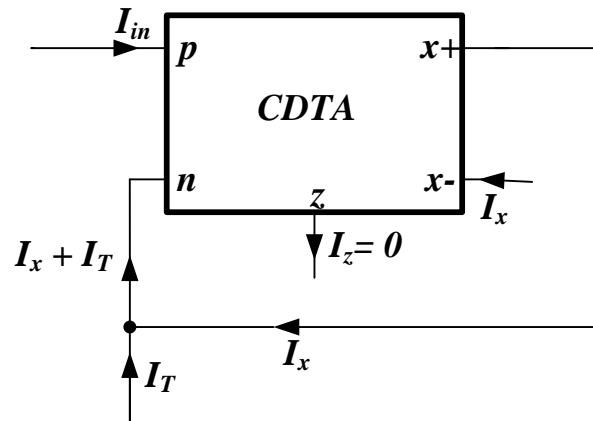


Fig. 3-25: Current summation using CDTA.

We let z node outlet open, thus

$$I_z = I_p - I_n, \quad I_z = 0 \quad (3-22)$$

$$I_p = I_n, \quad I_n = I_x + I_T$$

$$I_{in} = I_x + I_T$$

$$I_x = I_{in} - I_T \quad (3-23)$$

3.3.2. CMOS Implementation of CDTA

Fig. 3-26 shows CMOS bulk-driven CDTA implementation based on Fig. 3-23 (b).

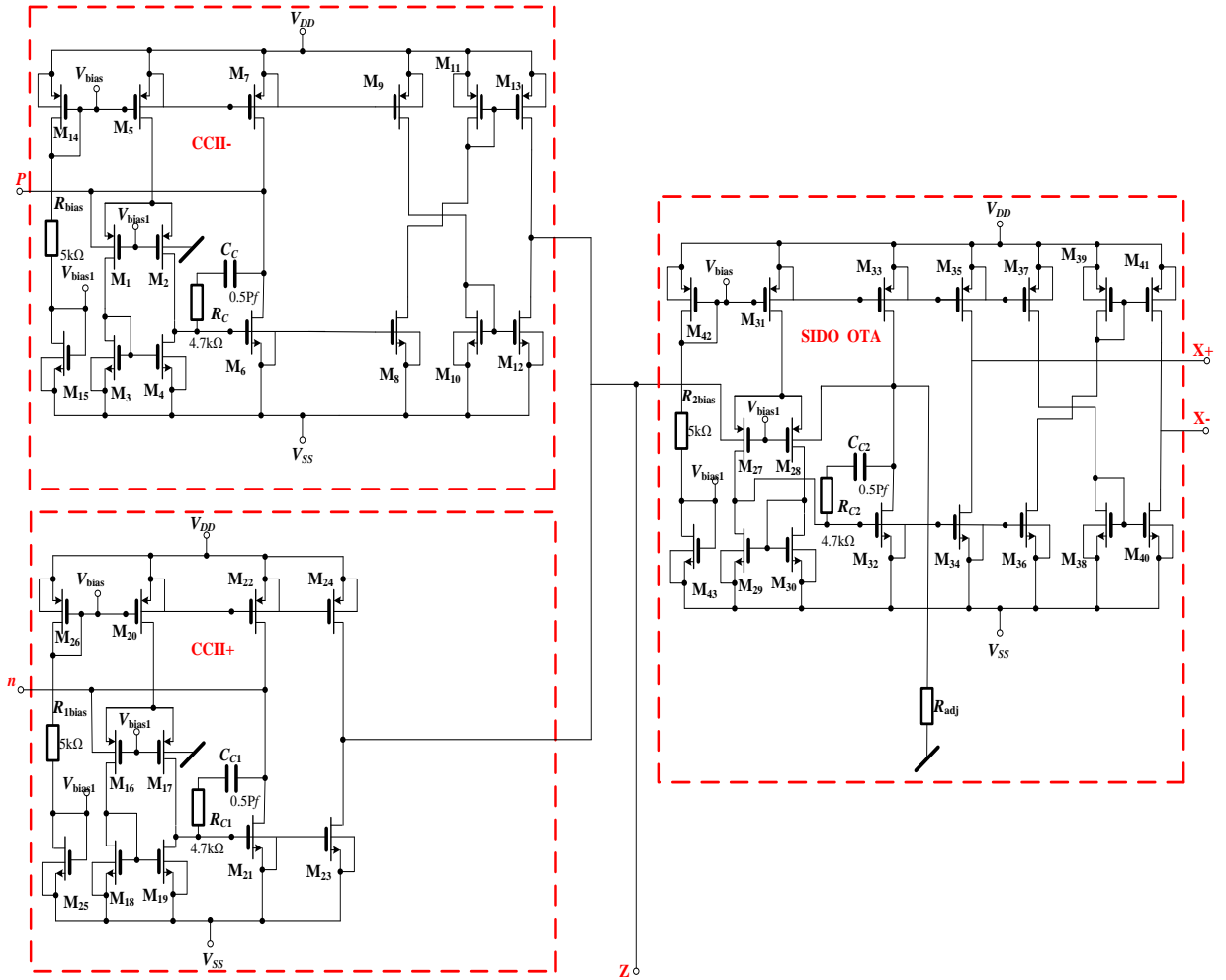


Fig. 3-26: CMOS implementation of CDTA.

The simulation results for the CDTA according to Fig. 3-26 are given in Figs. 3-27 to 3-32, and its small-signal parameters are summarized in Table 4-6.

Fig. 3-27 shows the I_z/I_p and I_z/I_n curves of the Current Differencing Unit (CDU), simulated on the assumption of $V_z = 0$. Note that for positive input currents I_p and I_n , the boundary of linear operation is ca 16 μ A. The current offset ΔI_z is ca -141 nA. For the bias point $I_p = I_n = 0$, the corresponding small-signal current gains are as follows: $\alpha_p = I_z/I_p = 0.986$, $\alpha_n = I_z/I_n = 1$.

The frequency responses of current gains I_z/I_p , I_z/I_n are given in Fig. 3-28. The cutoff frequencies for the gains α_p and α_n are 22 MHz and 75 MHz, respectively.

The voltage-current characteristic of the p -terminal input gate of the CDTA is shown in Fig. 3-29. Identical results also hold for the n -terminal. Note that when the input current approaches a value of ca 17 μ A, the clipping property of this curve can cause a significant nonlinear distortion. However, the range of linear operation is suitable for many applications that need extra low power consumption.

For the DC bias $I_p = 0$, the small-signal resistances R_p and R_n are 166 Ω . The frequency dependences of the impedances of p - and n - terminals in Fig. 3-30 show that the above values are kept up to ca one hundred kilohertz. Then the impedances increase due to the frequency dependence of the OTA transconductances.

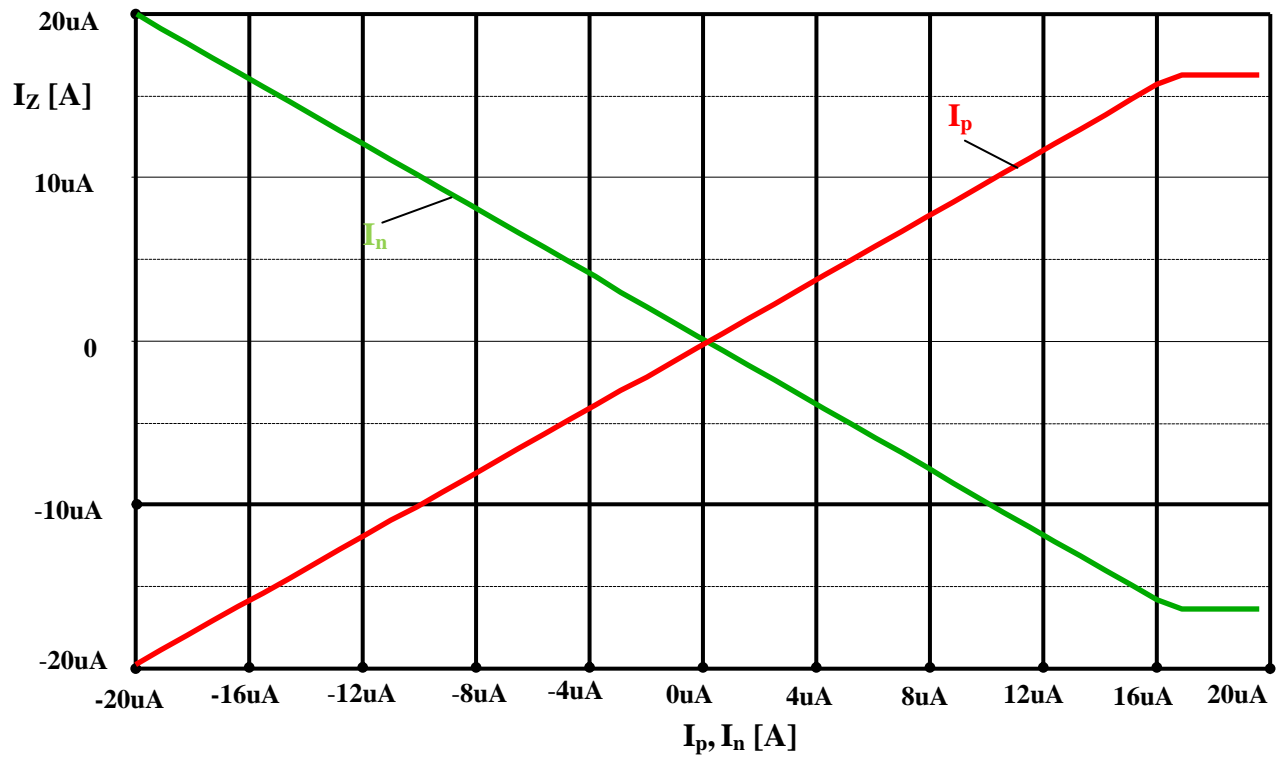


Fig. 3-27: DC curves I_z versus I_p or I_n , for $V_z = 0$.

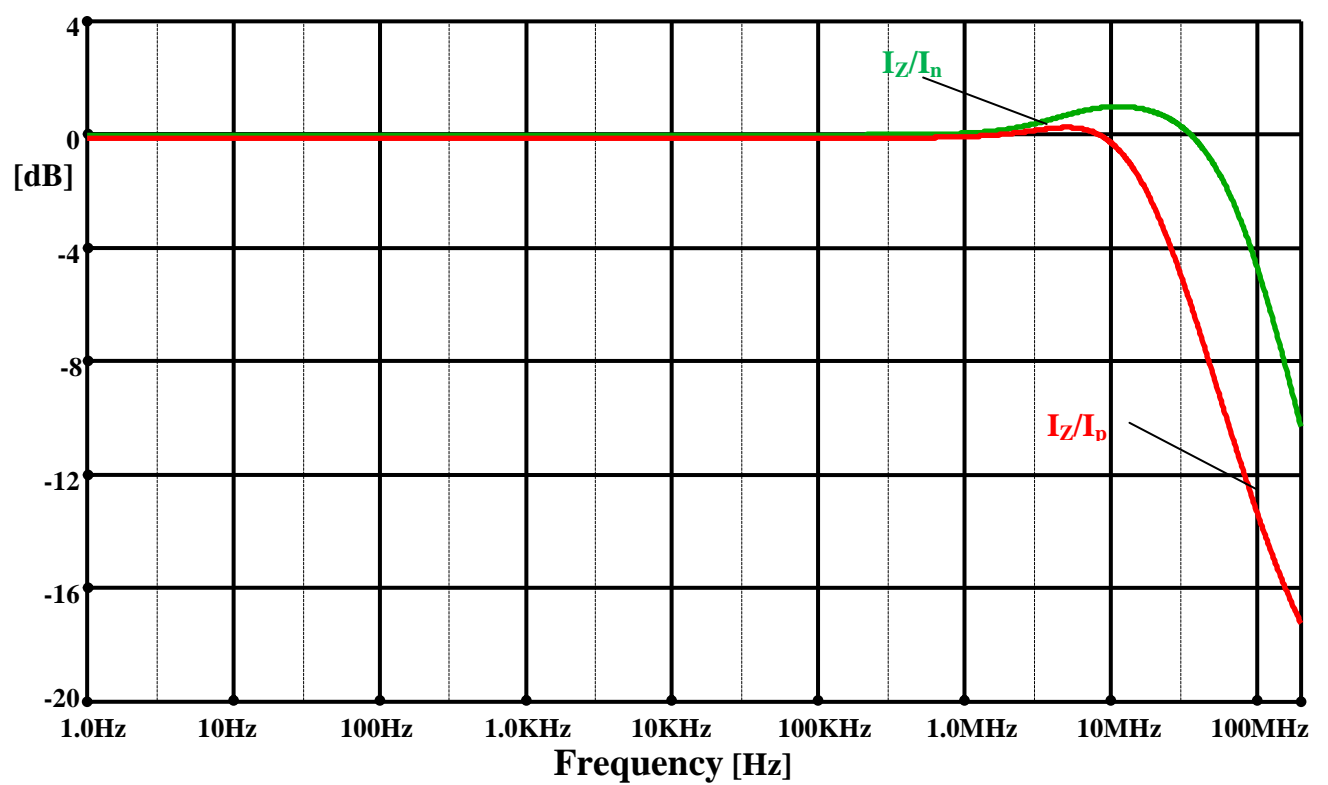


Fig. 3-28: Frequency responses of current gains I_z/I_p and I_z/I_n for $V_z = 0$.

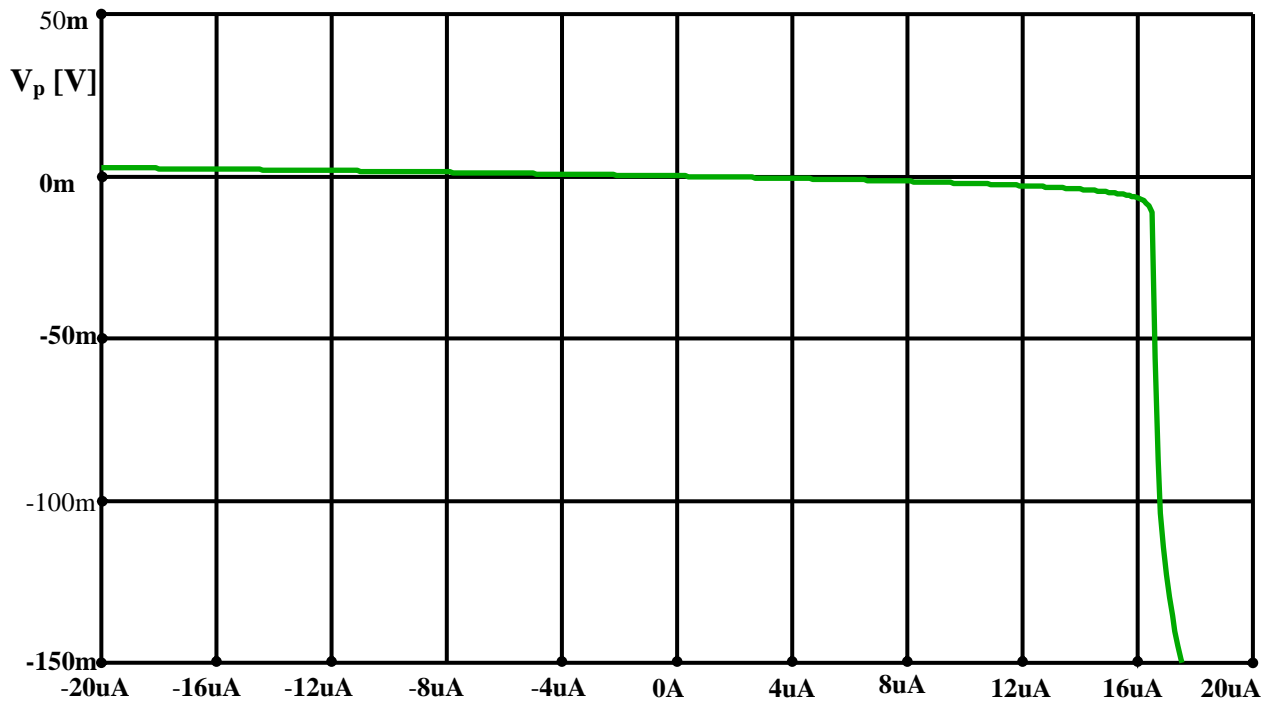


Fig. 3-29: DC curve V_p versus I_p for evaluating small-signal input resistance of the p-terminal. For the n-terminal, the result is identical.

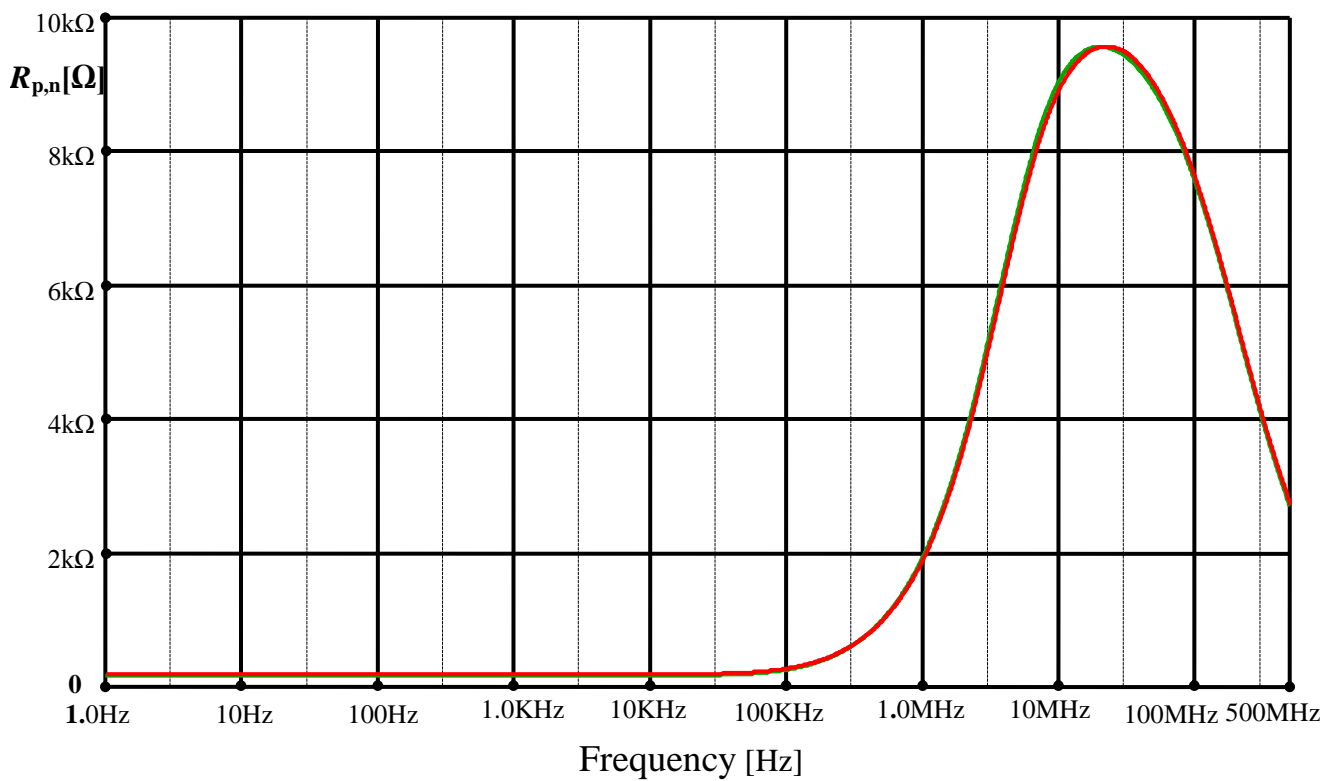


Fig. 3-30: Frequency dependence of the impedances of p- and n- terminals.

The I_x versus V_z curves in Fig. 3-31 are analyzed for several values of the external resistance R_{set} . They clearly show the transconductance control via R_{set} as well as the effect of the linearization and increasing the dynamic range with increasing values of R_{set} . A detailed analysis also confirms that the current offset is decreasing with increasing value of R_{set} . For $R_{set} = 10 \text{ k}\Omega$, the offset current is only -141 nA . Fig. 3-32 shows the frequency dependences of $g_{m,set}$ and of the x - and z -terminal impedances. The transconductance bandwidth increases with increasing R_{set} . For example, $R_{set} = 10 \text{ k}\Omega$ yields $g_{m,set} \approx 99 \text{ }\mu\text{A/V}$ and the -3dB cutoff frequency is approximately 1.1 MHz . The frequency dependence of the z -terminal impedance shows the value $277 \text{ k}\Omega$, with a -3dB cutoff frequency of about 2 MHz . The low-frequency x -terminal resistance is ca $554 \text{ k}\Omega$. Simulation results of the CDTA are summarized in Table 3-6.

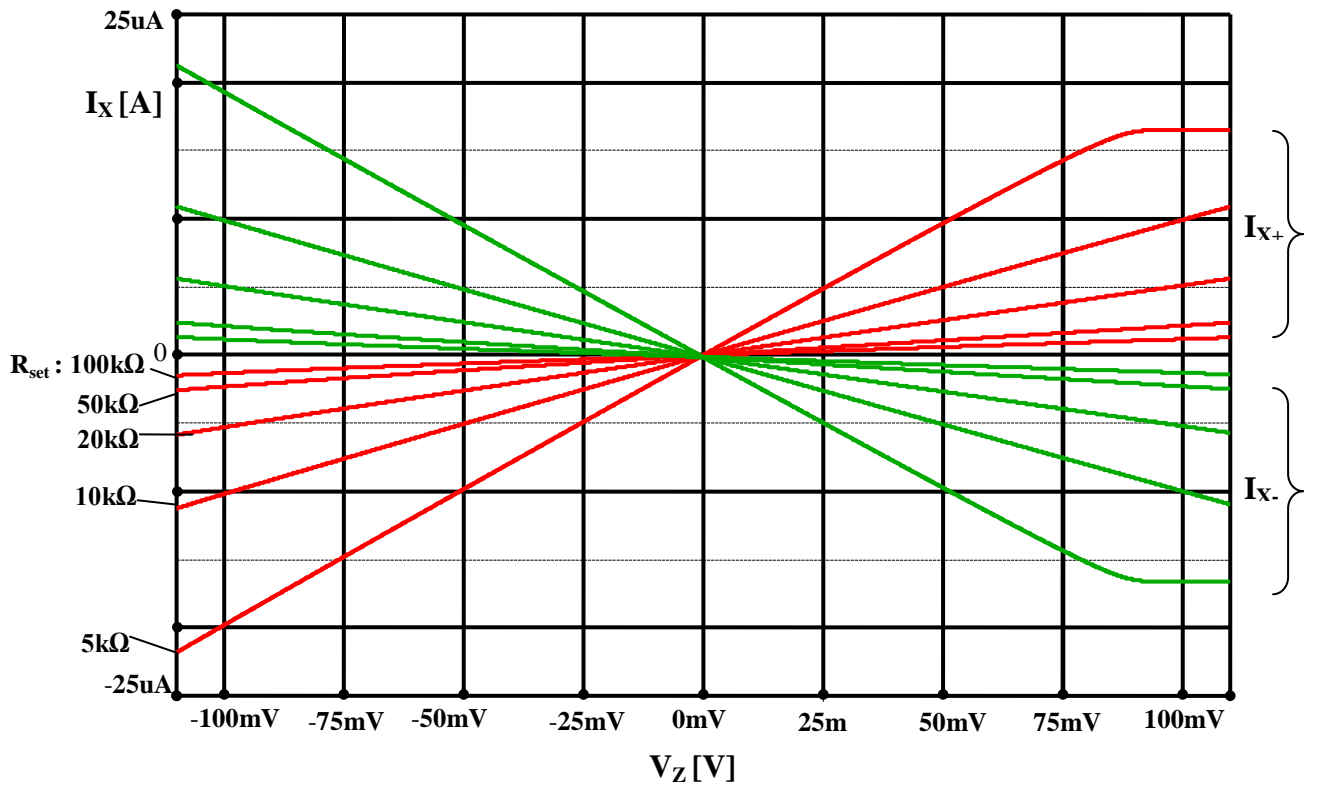


Fig. 3-31: DC characteristics of OTA No. 3 with R_{set} linearization and transconductance control.

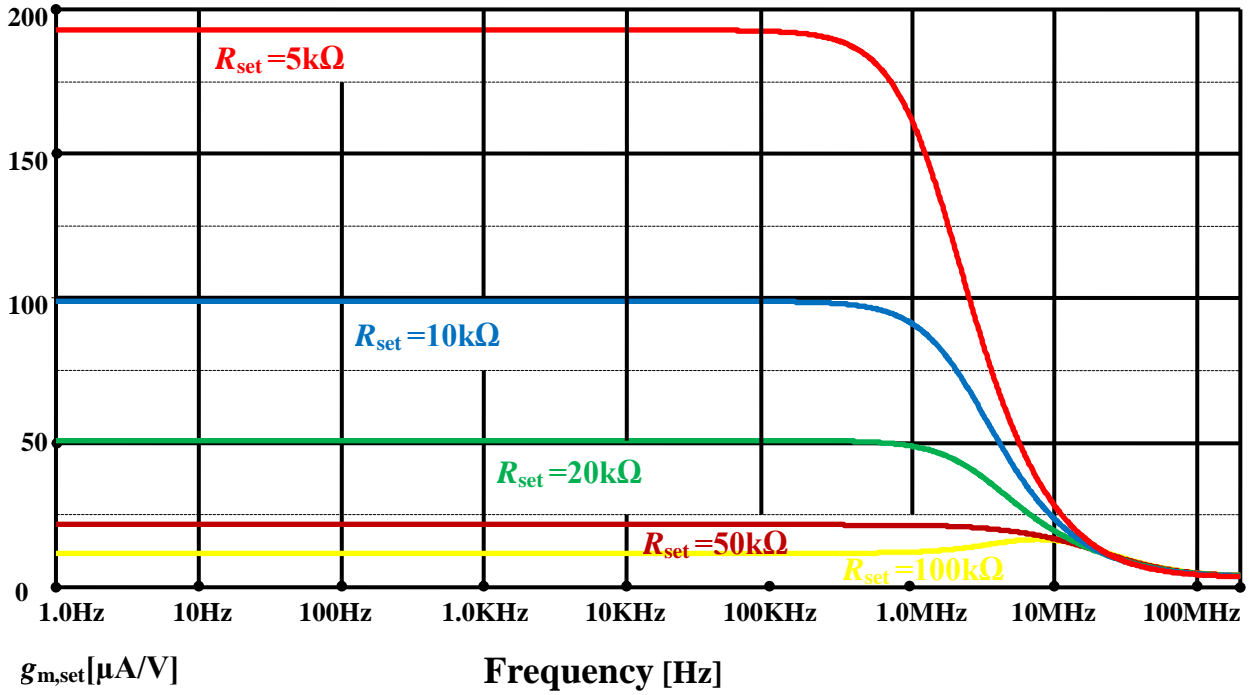


Fig. 3-32: Frequency responses of transconductances.

Characteristics	Simulation Result
Power consumption	264 μ W
3dB bandwidth I_Z/I_p , I_Z/I_n	22 MHz, 75MHz
DC current range I_p , I_n	± 16 μ A
DC voltage range V_Z ($R_{set} = 10k\Omega$)	+170 mV, -310 mV
DC offset of OTA stage ($R_{set} = 10k\Omega$)	-141 nA
Current gains I_Z/I_p , I_Z/I_n	0.986, 1
g_m ($R_{set} = 10k\Omega$)	98.9 μ A/V
3dB bandwidth g_m ($R_{set} = 10k\Omega$)	1.2 MHz
Node n and p parasitic DC resistance	166 Ω
Node z parasitic DC resistance	277 k Ω
Node x parasitic DC resistance	554 k Ω
Measurement condition: $V_{DD} = 0.6V$, $V_{SS} = 0.6V$	

Tab. 3-6: Simulation results of the Bulk-driven CDTA.

3.4. Voltage Differencing Transconductance Amplifier (VDTA)

The methodology described in the CDTA, which uses the CDU as the input unit, and the following simple block OTA represents an open system: Let us continue with the variation that the input unit will now implement voltage and not current differences. The differential-input OTA is a simple element for realizing the voltage difference. Simultaneously, it can

provide the possibility of electronic control. The VDTA element [23] with its schematic symbol in Fig. 3-33 (a) has a pair of high-impedance current inputs p and n , and an auxiliary terminal z . A multiple copies of I_z current are indicated here in order to increase the universality of VDTA element. Thus, according to the proposed methodology, the VDTA element should have the “zc“(Z Copy) attribute. Also a possible implementation of VDTA using two OTA components is given in Fig. 3-33 (b). Here, output terminal currents are equal in magnitude, but flow in opposite directions, and the product of transconductance (g_m) and the voltage at the z terminal gives their magnitudes. Therefore, this active element can be characterized with the following equations:

$$I_p = I_n = 0, \quad I_z = g_{mz}(V_p - V_n) \quad (3-24)$$

$$I_{zc} = \pm I_z \quad (3-25)$$

$$I_{x+} = g_{mx}V_z, \quad I_{x-} = -g_{mx}V_z \quad (3-26)$$

VDTA has an interesting application potential: for example, the floating loss-less inductor can be simulated only by one VDTA and one grounded capacitor.

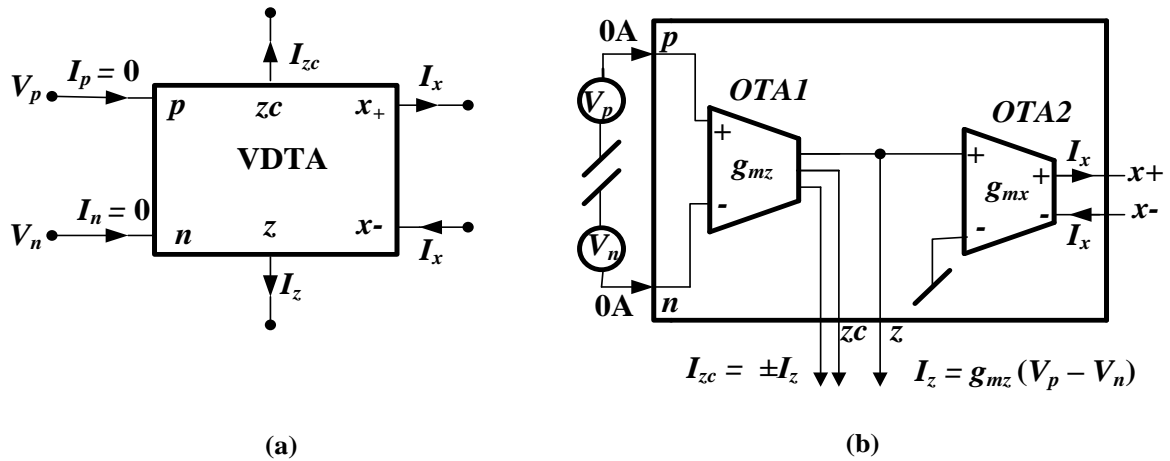


Fig. 3-33: (a) Symbol of the VDTA, (b) its implementation by OTAs.

3.4.1. Operations using the ideal VDTA

- **Integrator using VDTA**

The operation of integration can be achieved very conveniently using the VDTA as is shown in Fig. 3-34. Clearly,

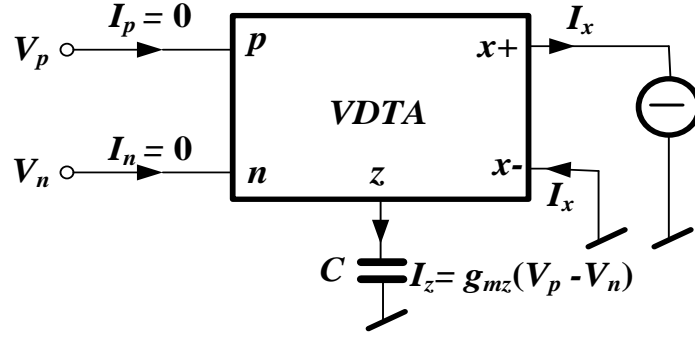


Fig. 3-34: Integrator using VDTA.

$$I_z = g_{mz}(V_p - V_n) \quad (3-27)$$

$$V_z = \frac{I_z}{sC} = \frac{g_{mz}(V_p - V_n)}{sC}$$

$$I_x = g_{mx}V_z = \frac{g_{mx}g_{mz}(V_p - V_n)}{sC}$$

$$\frac{I_x}{(V_p - V_n)} = \frac{g_{mx}g_{mz}}{sC} \quad (3-28)$$

- **Current Summation using VDTA**

Current summation can be obtained using VDTA as shown in Fig. 3-35.

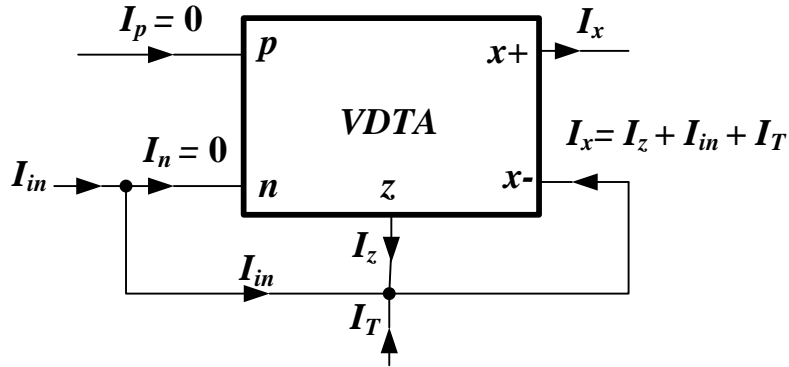


Fig. 3-35: Current summation using VDTA.

3.4.2. CMOS Implementation of VDTA

For low-voltage low-power applications, it can be advantageous to implement the VDTA element in Fig. 3-33 (b) with the utilization of bulk-driven [82] CMOS technique. One possibility is presented in Fig. 3-36.

VDTA is built here by means of two OTAs of DISO (Differential Input Single Output) and SIDO (Single Input Differential Output) types. This circuit uses low supply voltages, namely ± 0.6 V. The total power dissipation is less than $206\mu\text{W}$.

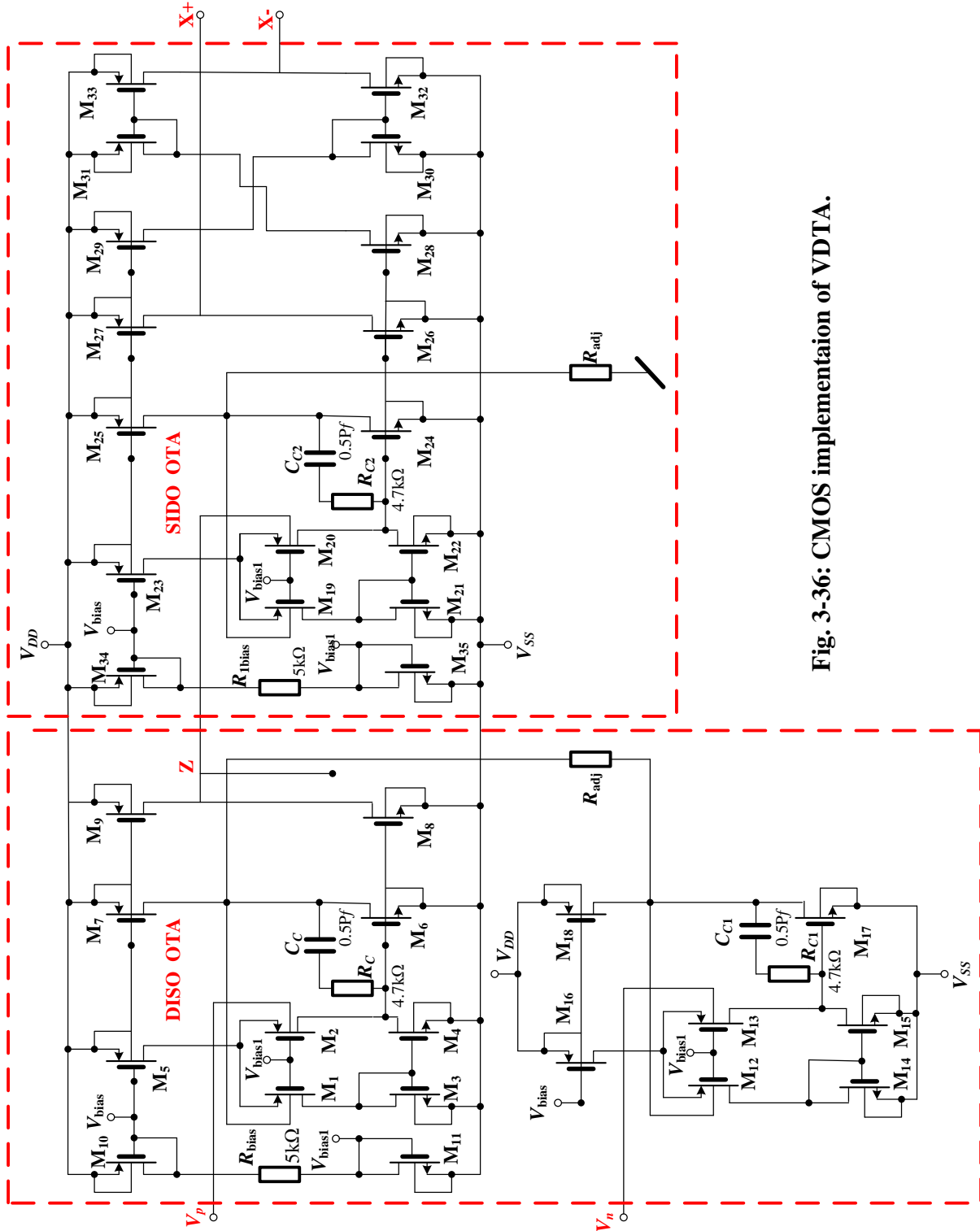


Fig. 3-36: CMOS implementation of VDTA.

3.5. Voltage Differencing Voltage Transconductance Amplifier (VDVTA)

The VDVTA element [23] with its schematic symbol in Fig. 3-37 (a), and in Fig. 3-37 (b) is given with a possible implementation using two OTA components (Differential Input Single Output DISO and Differential Input Differential Output DIDO).

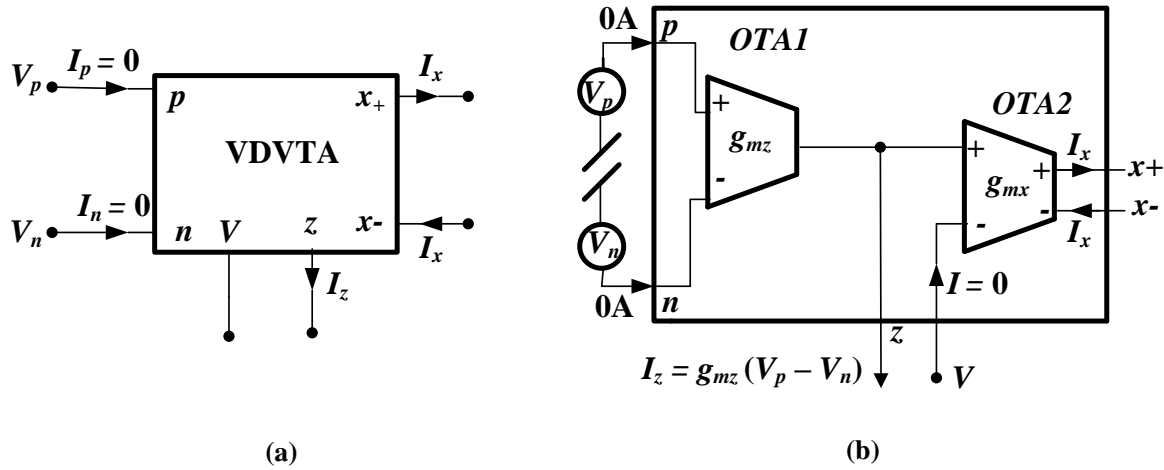


Fig. 3-37: (a) Symbol of the VDVTA, (b) its implementation by OTA.

For low-voltage low-power applications, it can be advantageous to implement the above element with the utilization of bulk-driven [82] CMOS technique.

Fig. 3-38 shows CMOS bulk-driven implementation of Fig. 3-37 (b) utilizing DISO (Differential Input Single Output) and DIDO (Differential Input Differential Output) OTA implementations. This circuit uses low supply voltages, namely ± 0.6 V. The total power dissipation is less than $206\mu\text{W}$.

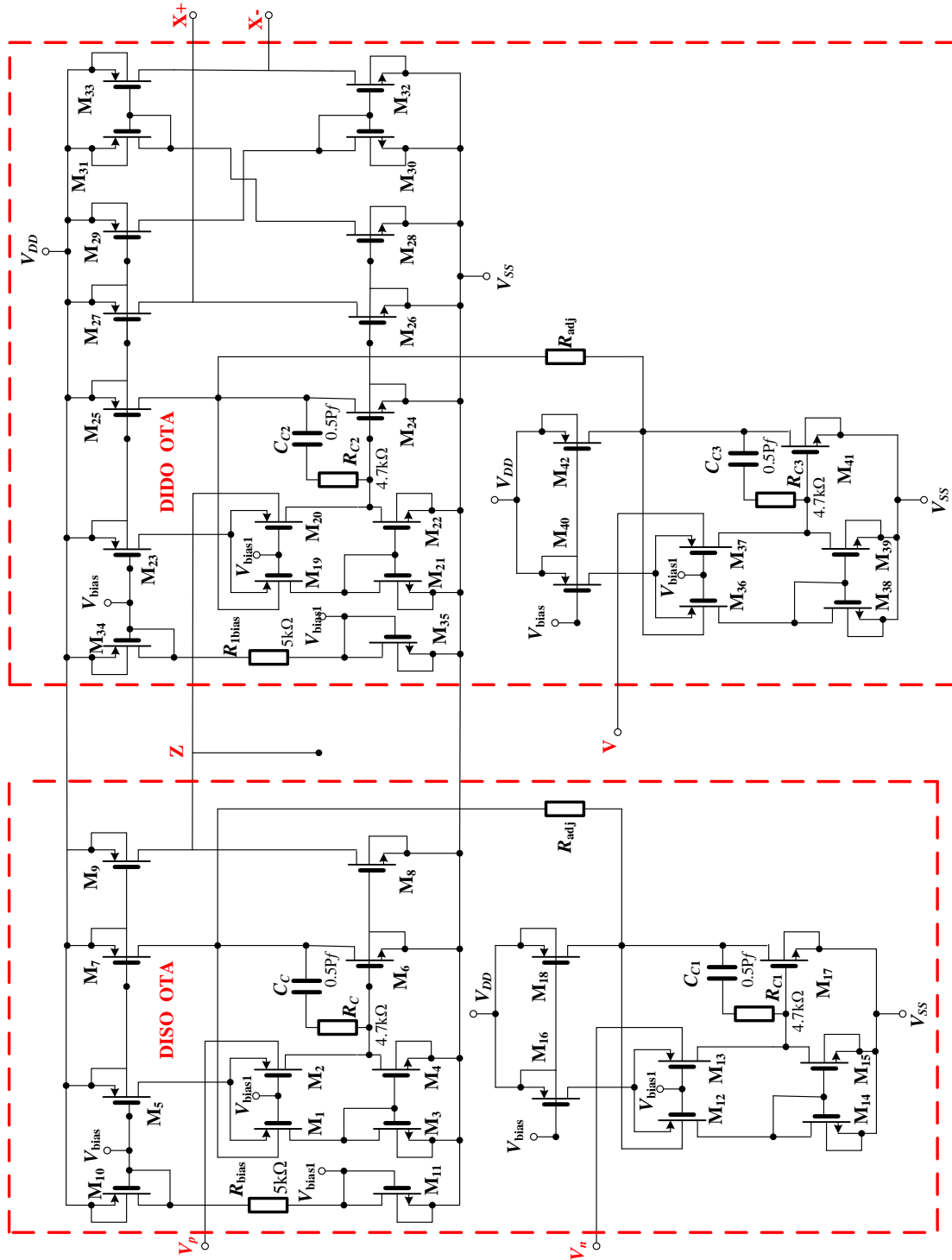


Fig. 3-38: CMOS implementation of VDVTA.

3.6. Differential Voltage Current Conveyor (DVCC)

Since its first introduction by A. Sedra and K. Smith in 1970 [6], the second-generation current conveyor (CCII) has proved to be a versatile analog building block that can be used to implement numerous high frequency analog signal applications, like filters and current-mode oscillators. However, when it comes to applications demanding differential or floating inputs

like impedance converter circuits and current mode instrumentation amplifiers, which also require two high input impedance terminals, a single CCII block is no more sufficient.

In addition, most of these applications employ floating elements in order to minimize the number of used CCII blocks. For this reason and in order to provide two high input impedance terminals, two active building blocks, namely, the differential voltage current conveyor (DVCC) and the differential difference current conveyor (DDCC) have been proposed in the late 90s.

The DVCC is a five-port building block which is defined by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y+} \\ I_{Y-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y+} \\ V_{Y-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (3-29)$$

A symbol of DVCCII building block and its implementation by Diamond Transistors (DT) are shown in Fig. 3-39 [1].

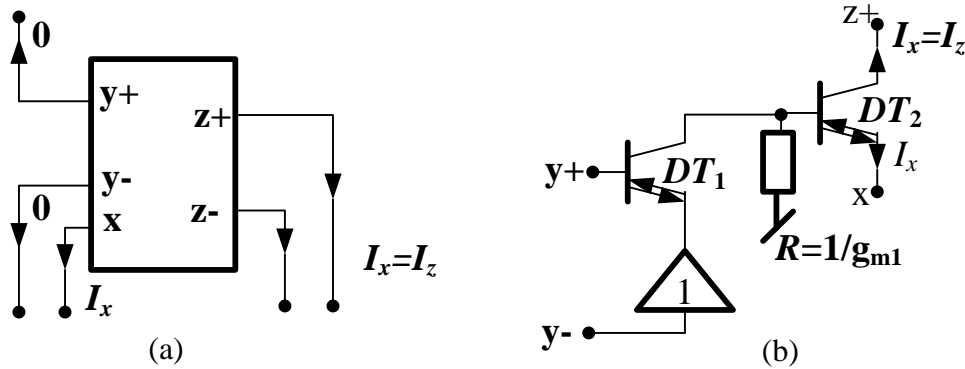


Fig. 3-39: (a) DVCCII+ model, (b) DVCCII+ using diamond transistors and buffer.

Note that DT can be simply applied as SISO (Single-Input Single-Output) OTA. DISO (Differential Input Single Output) OTA implementation requires an additional voltage buffer in order to provide high-impedance inverting input. The implementation of DVCCII by DISO (Differential Input Single Output) OTA and Current Conveyor second generation CCII is shown in Fig. 3-40.

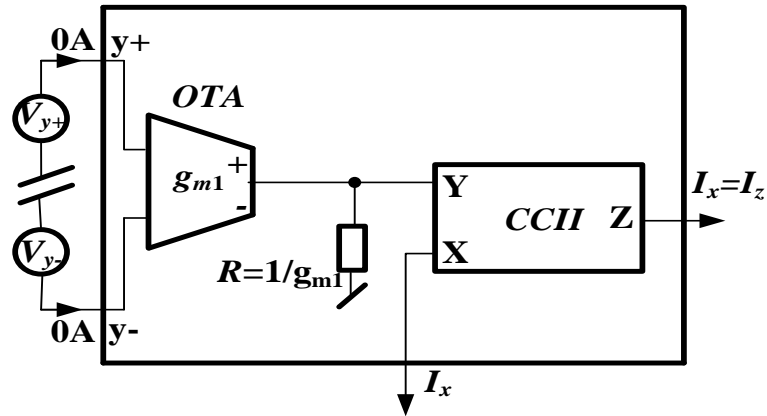


Fig. 3-40: Implementation of DVCII+ by current conveyor and by OTA.

Fig. 3-41 shows CMOS bulk-driven implementation of circuit idea in Fig. 3-40 utilizing DISO (Differential Input Single Output) OTA CCII.

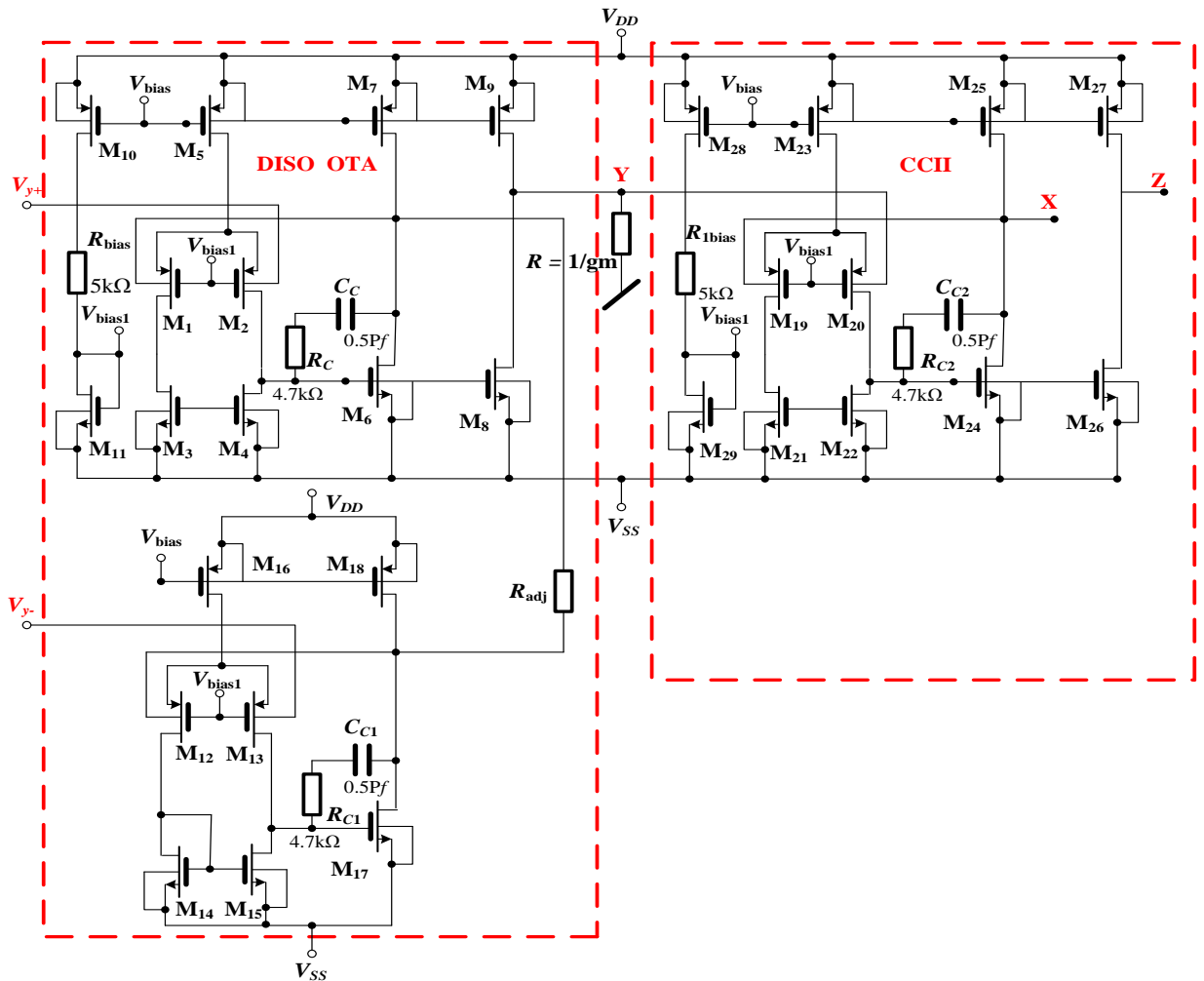


Fig. 3-41: CMOS Implementation of DVCII+ by Bulk-driven current conveyor and by OTA.

4. LC ladder simulation and other applications of active elements

4.1. Optimization of ladder filters with GmC simulation of floating inductors

Replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design. An efficient way of simulating the floating inductor consists in replacing the inductor by three OTAs (Operational Transconductance Amplifier) and one grounded capacitor [51]. However, the common drawback of OTAs is the low-level input voltage providing the linear mode of the amplifier.

This can be in conflict with the requirements for a large dynamic range of signals being processed. When the filter is designed for the current-mode, the current limitations of the active elements should also be carefully monitored.

MAX435 is a commercial OTA [57], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well known circuitry for simulating the floating inductor [51]. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.

Using the concrete example of 5th-order video filter, a method for designing and optimizing such a circuit is described in this paper. The commercial MAX435 is used in the subcircuits of synthetic inductances. The procedure described can be applied to an arbitrary type of OTA.

4.1.1. MAX435 – a commercial OTA

MAX435 is an OTA with 275MHz bandwidth and 850V/us slew rate. Its recommended symmetrical power supply is $\pm 5V$. The transconductance g_m is set within a wide range by means of auxiliary R_t resistor [57]. The recommended maximum current through R_t as well as the output current are 10mA. A concrete saturation level I_{max} can be adjusted by R_{set} resistance approximately from 3mA up. $R_{set} = 5.9k\Omega$ corresponds to a current of 10mA. The maximum recommended differential voltage is 2.5V.

4.1.2. Synthetic inductor based on MAX435

Fig. 4-1 shows a synthetic floating inductor which employs a pair of differential-input differential-output OTAs. It is a generalization of the circuit from [51], where three single-

output OTAs are used for inductor replacement. The signal flow graphs attached describe the process of transforming voltage V_1 into current I_1 of OTA No. 1, transforming current I_1 into voltage across the capacitor, and transforming capacitor voltage into current I_2 .

It follows from the last graph that the circuit implements a lossless floating inductor with the inductance

$$L = \frac{C_L}{g_{m1}g_{m2}} \quad (4-1)$$

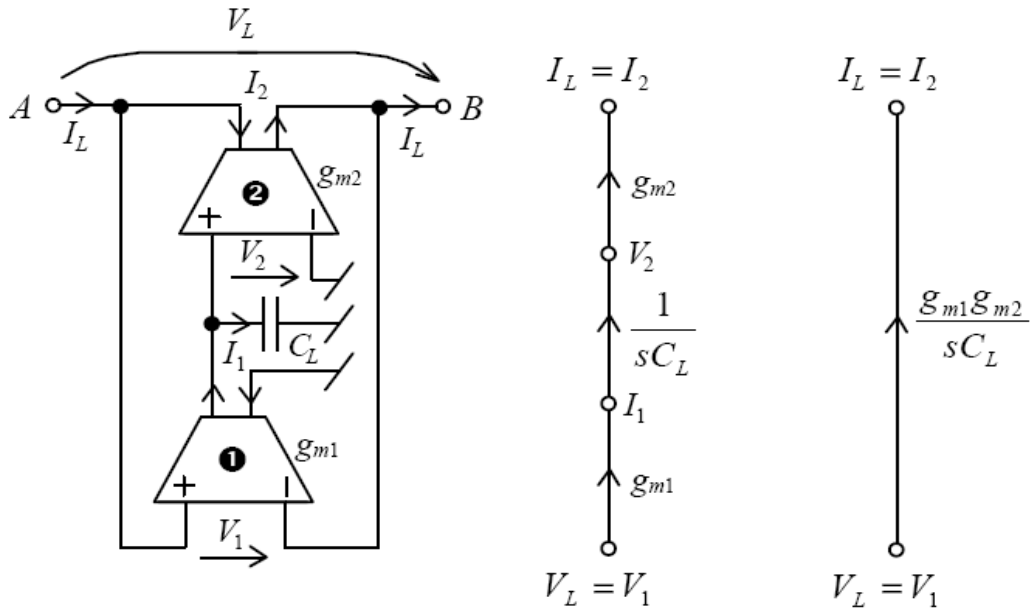


Fig. 4-1: Synthetic inductor and the corresponding signal flow graphs.

There are two degrees of freedom when designing the transconductance g_{m1} and g_{m2} and the capacitance C_L from the desired inductance value. They can be used for dynamic range optimization. The following rule results from 4-1:

The inductor is preliminarily designed with the parameters g_{m1} , g_{m2} , and C_L . These parameters will be modified according to the rule

$$C'_L = a_0 C_L, \quad g'_{m1} = a_1 g_{m1}, \quad g'_{m2} = a_2 g_{m2} \quad (4-2)$$

Where a_0 , a_1 , and a_2 are real positive numbers, fulfilling the equality

$$a_0 = a_1 a_2 \quad (4-3)$$

Then the resulting inductance is not changed due to this modification. However, current I_1 will be a_1 times greater and voltage V_2 will be a_1/a_0 times greater than before the modification of the parameters.

This rule will be used for the dynamic range optimization of target application, i.e. the active filter which simulates the LC ladder.

The following equality also results from the graph in Fig. 4-1:

$$\frac{V_2}{V_1} = \frac{g_{m1}I_2}{g_{m2}I_1} \quad (4-4)$$

The purpose of optimizing the upper limit of the dynamic range is to equalize the voltage and current levels inside the synthetic inductors, thus $V_1 = V_2$ and $I_1 = I_2$. Eq. 5-1 shows that a complete equalization is enabled only when both transconductances are equal.

4.1.3. LC Ladder simulation

Fig. 4-2 shows the schematic of a low-pass LC ladder filter which has been designed according to Bessel approximation on the basis of the following specifications:

DC gain 0dB, 3-dB cutoff frequency 5MHz, attenuation at least 50dB for frequencies above 27MHz, maximally flat group delay. This specification is derived from the parameters of commercial video filter FMS6400-1 by Fairchild Semiconductor [58].

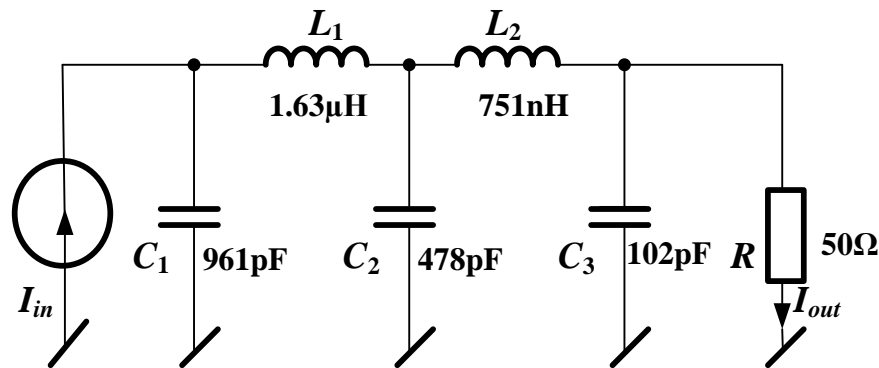


Fig. 4-2: 5MHz low-pass ladder filter.

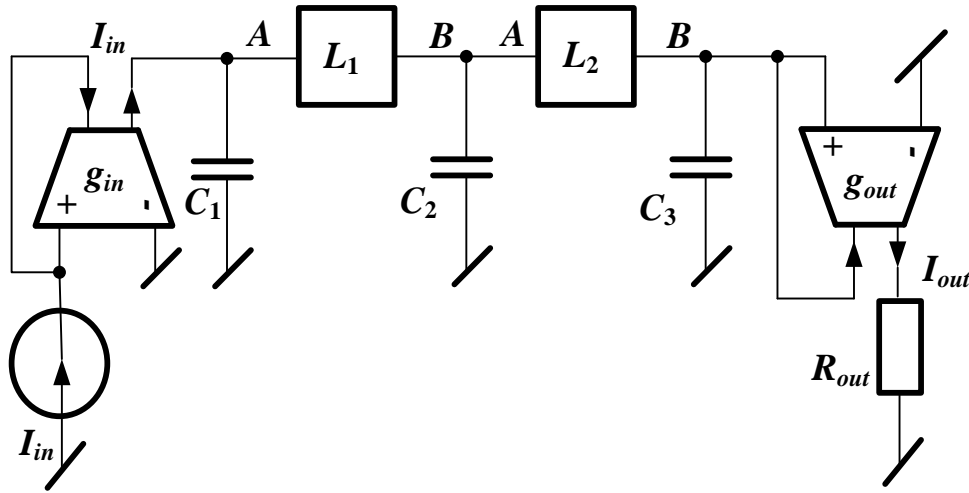


Fig. 4-3: Active ladder simulation by means of synthetic inductors and OTAs.

An active realization of the LC ladder is shown in Fig. 4-3. Blocks “ L_1 ” and “ L_2 ” are the synthetic inductors from Fig. 4-1. OTA with transconductance g_{in} serves as a current-controlled current source, providing low driving point impedance $R_{in} = 1/g_{in}$ for the input current source.

OTA with transconductance $g_{out} = 1/R = 20\text{mS}$ delivers current I_{out} into an independent load R_{out} .

Let us design the active filter from Fig. 4-3 for a maximum driving current value of 10mA. The results of PSpice AC analysis of the passive LC ladder from Fig. 4-2 are shown in Fig. 4-4. The analysis was performed on the assumption of the attribute AC=10mA of the current source I_{in} . Those curves are depicted which are important for studying the filter dynamic range, i.e. the output voltage across R (i.e. the input voltage of the terminating OTA), the output current through R (i.e. the output current of the terminating OTA), the voltages across L_1 and L_2 (i.e. the input voltages of OTA No. 1 in the synthetic inductors from Fig. 4-1), and the currents through L_1 and L_2 (i.e. the output currents of OTA No. 2 in the synthetic inductors from Fig. 4-1). The curves are determined by the parameters of filter elements and they can be influenced only via choosing another realization structure, another approximation of frequency response or another impedance level. The Bessel approximation used here guarantees a maximally flat group delay response.

Fig. 4-4 shows that both the synthetic inductors and the terminating OTAs should be designed for a maximum current of 10mA. It is fulfilled for MAX435 when adjusting $R_{set} = 5.9\text{k}\Omega$. The input voltage of the end OTA is maximum (1V) for low frequencies. The required

g_m value of this OTA is $1/R = 20\text{mA/V}$ and it can be set via $R_t = 200\Omega$ [57]. This amplifier will operate in the linear regime till its full current excitation.

The front-end OTA, excited by the current source I_{in} , will be designed with $g_{in} = 100\text{mA/V}$ or $R_t = 40\Omega$ in order to provide low driving point impedance $R_{in} = 1/g_{in} = 10\Omega$. The maximum value of the input voltage will be 100mV for full current excitation of the filter input.

The curves $V(L_1)$, $V(L_2)$, $I(L_1)$, and $I(L_2)$ can be used for designing the synthetic inductors. The voltage across L_1 (L_2) takes its maximum value 408mV (173mV) at a frequency of 6.31MHz (5.75MHz). As stated before, the currents are maximum, i.e. 10mA at a frequency of 0Hz .

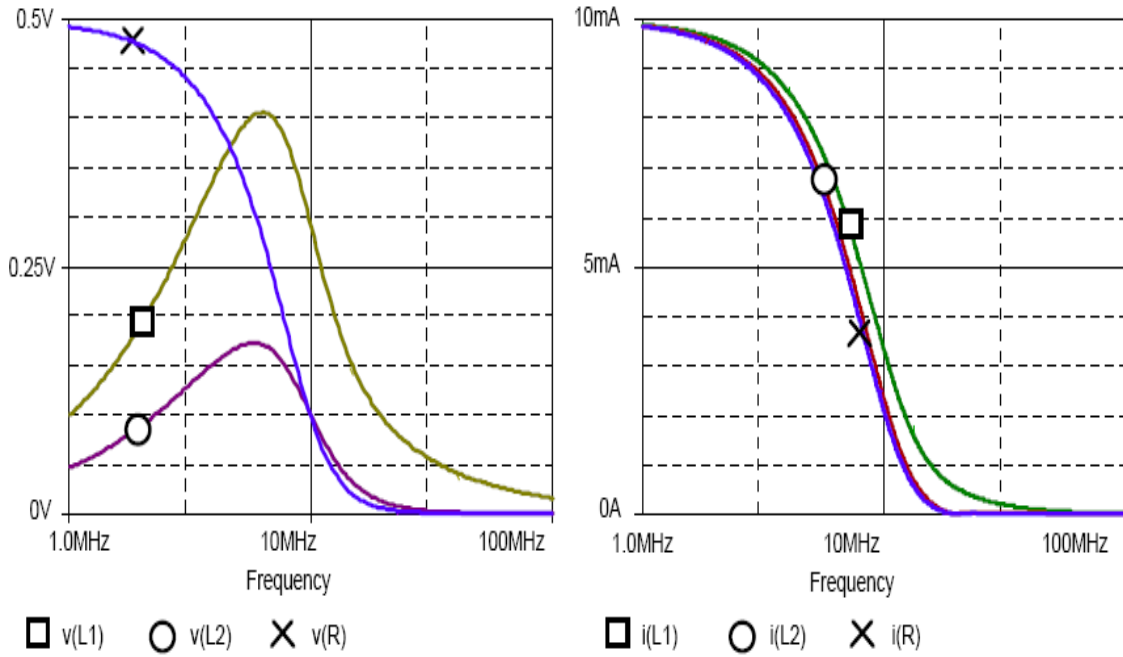


Fig. 4-4: Results of the AC analysis of LC ladder from Fig. 4-2 (a) for $I_{in} = 10\text{mA}$.

In the first step, a preliminary design of the synthetic inductors according to Eq. 4-1 will be performed. The initial capacitance in both inductors will be set to 100pF . For equal values of g_{m1} and g_{m2} , Eq. 4-1 leads to the results in Table 4-1.column (1).

		(1) Before optimization	(2) After optimization
L_1	g_{m1} [mA/V]	7.833	24.505
	g_{m2} [mA/V]	7.833	24.505
	R_{t1} [Ω]	511	163
	R_{t2} [Ω]	511	163
	C_L [pF]	100	979
L_2	g_{m1} [mA/V]	11.539	57.902
	g_{m2} [mA/V]	11.539	57.902
	R_{t1} [Ω]	347	69
	R_{t2} [Ω]	347	69
	C_L [pF]	100	2518

Tab. 4-1: Parameters of elements of the synthetic inductors before and after optimization.

The Signal-Flow-Graph from Fig. 4-1 describes relations among the internal variables of the synthetic inductor, particularly between the inductor terminal voltage, the output current of OTA No. 1, the input voltage of OTA No. 2, and the inductor terminal current. These relations can be pre-set in the Probe postprocessor of PSpice simulator [59]. The results are shown in Fig. 4-5(a). The left-side part contains the curves of OTA input voltages; the right-side shows the curves of OTA output currents.

The maximum values of voltages and currents from Fig. 4-5 are given in Table 4-2, column (1). Note that the input voltages of OTA No. 2 are too high whereas the output currents of OTA No. 1 do not reach their permitted maxima for either inductor. In addition, the following equality is true:

$$\frac{V_2}{V_1} = \frac{g_{m1}I_2}{g_{m2}I_1} \quad (4-5)$$

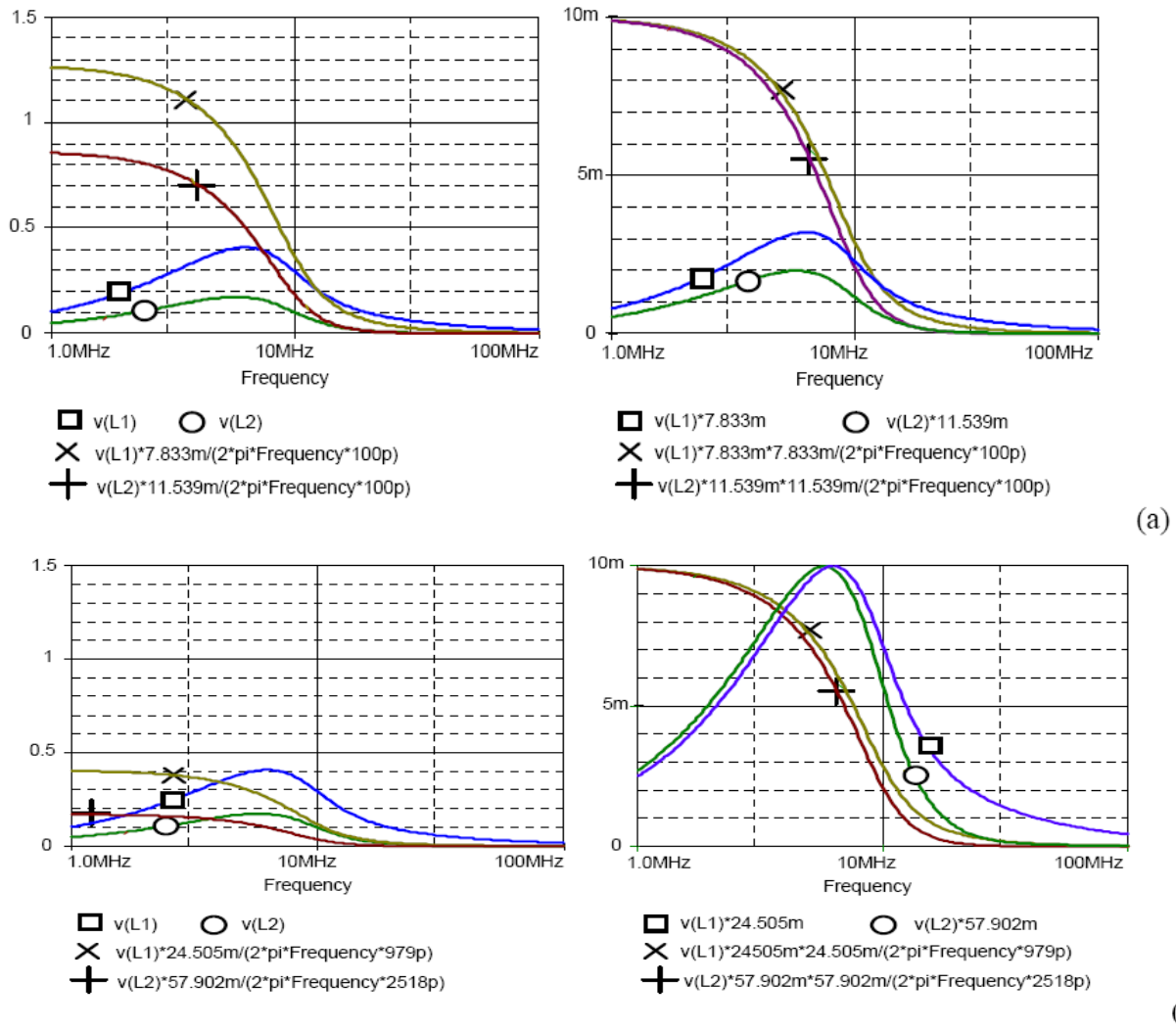


Fig. 4-5: PSpice analysis of synthetic inductors by means of dependences described by Signal- Flow-Graphs from Fig. 4-1, (a) before, (b) after optimizing the dynamic range.

		(1) Before optimization	(2) After optimization
L_1	$V_{1\max}$ [V]	0.4082	0.4082
	$V_{2\max}$ [V]	1.277	0.4082
	$I_{1\max}$ [mA]	3.197	10.003
	$I_{2\max}$ [mA]	10	10
L_2	$V_{1\max}$ [V]	0.1727	0.1727
	$V_{2\max}$ [V]	0.8666	0.1727
	$I_{1\max}$ [mA]	1.992	9.998
	$I_{2\max}$ [mA]	10	10

Tab. 4-2: Maximum values of inductor voltages and currents before and after optimization.

It is in conformity with Eq. (4-2). These ratios are 3.128 for inductor No. 1 and 5.018 for inductor No. 2.

Applying the rule from Section 4.1.2 and the corresponding equations (4-2) and (4-3), we conclude that the upper limits of the dynamic ranges of voltages and currents in the inductors can be equalized if both transconductance are multiplied by ratio 4/5 and the capacitance is simultaneously multiplied by the square of this ratio. After this optimization, the parameters of the elements are as shown in Table 4-1, column (2). The corresponding frequency responses are given in Fig. 4-5 (b) and the maximum values of voltages and currents can be found in column (2) of Table 4-2.

Frequency responses of the optimized active filter, simulated in PSpice simultaneously with the frequency responses of ideal LC ladder, are shown in Fig. 4-6. Note that the group delay is more sensitive to real properties of the amplifiers than the gain response. The analysis found that low output impedance of MAX435, namely $3.5k\Omega$, is a dominant factor which imports losses to the ladder structure. Nevertheless, the group delay ripple is less than is specified for similar commercial video filter FMS6400-1 [58].

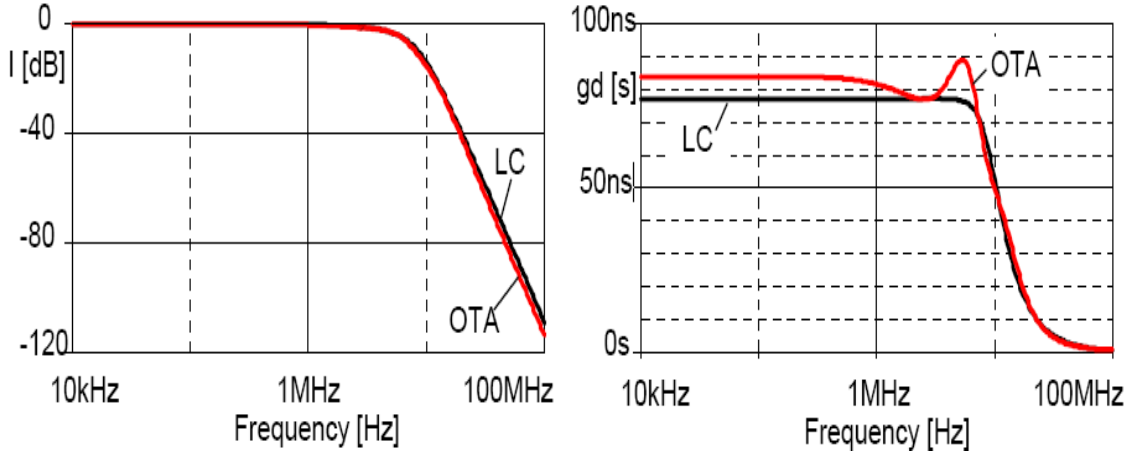


Fig. 4-6: Frequency responses of ideal LC ladder (LC) and optimized active filter.

4.2. Commercial active elements for filter implementation

The OTAs belong to the most popular active components for LC ladder simulation [60]; see Fig. 4-7 (a). Several circuits are used for simulating the floating inductor. The most economical one consists of a pair of OTAs and one grounded capacitor, one of them having a single-input and a differential output, the other a differential input and a single output. An interesting commercial element which would be optimal for such implementation was MAX 435 by MAXIM corporation [57]. However, its manufacturing was terminated. The well-known OTA LM13700 by National Semiconductor [61] has a differential input and a single output. However, its bandwidth (2MHz) is too low for video signal processing.

It is well known that OTA can be implemented by the CCII: the high-impedance y terminal is used for voltage excitation. The low-impedance x terminal is grounded. The current, flowing through the x terminal into the ground, is equal to the input voltage divided by the internal resistance R_x of the x terminal. This current is copied by an internal current mirror onto the z terminal. Such a circuit then acts as the single-input single-output OTA with transconductance $g_m = 1/R_x$. When utilizing the current-controlled CCII (CCCII) [62], the transconductance can be controlled electronically by an external quiescent current.

The so-called “diamond transistor” OPA660 [63] by Burr Brown/Texas Instruments belongs to the well-known commercial CCCIs. However, today it is an obsolete product. Its analogy is available in the form of perspective circuits OPA615, SHC615, OPA860, and OPA861 from the above company. All of them contain the S-T, or – in other words – the CCCII whose intrinsic R_x resistance is adjustable by an external current. In addition, OPA860 contains a very fast and independently utilized voltage buffer, whereas OPA615 and SHC615 include a fast comparator in the form of differential input single output OTA with extremely high transconductance.

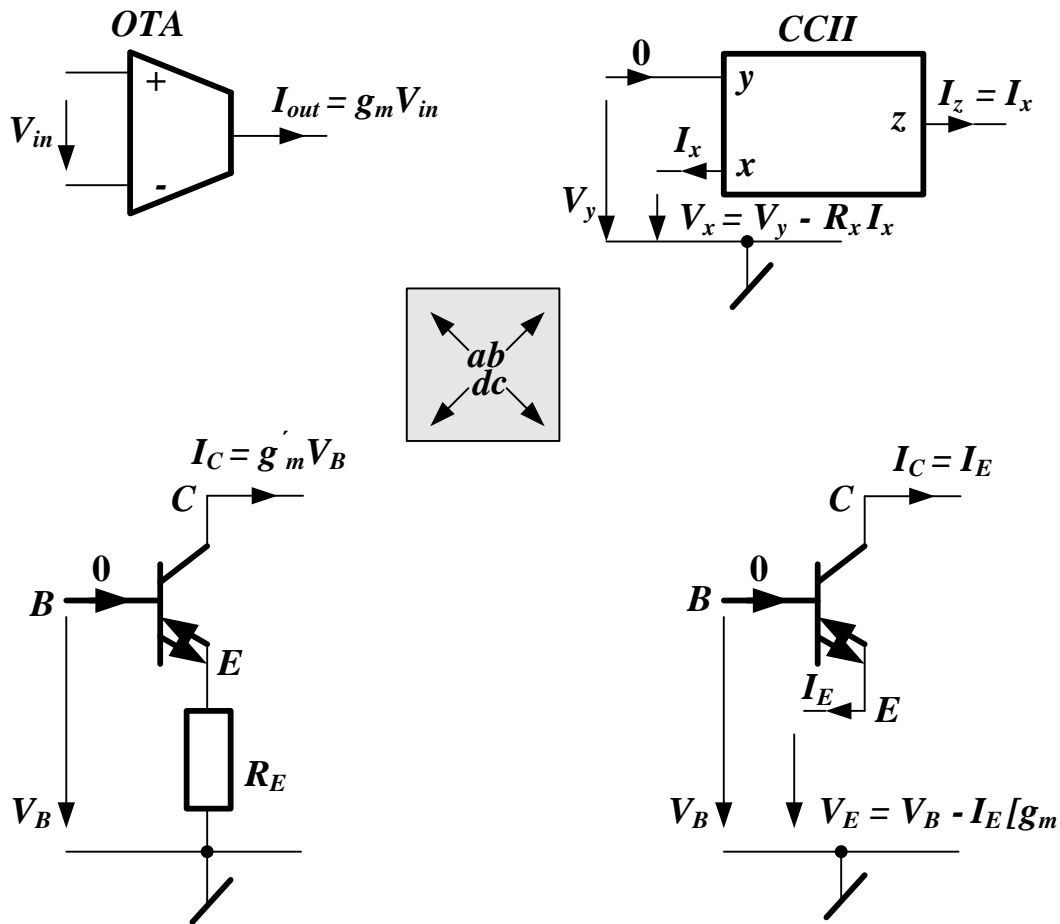


Fig. 4-7: (a) OTA, (b) CCII with nonzero x-terminal resistance, (c) „super-transistor“ as CCII, (d) „super-transistor“ with a degeneration R_E resistance as single-input single-output OTA.

The “super-transistors” also have comparatively high transconductances (up to 100 mA/V) and their characteristic $I_{out} = f(V_{in})$ is rather nonlinear; thus the linear operation region is within the V_{in} range of tens of millivolts. This drawback, which prevents this element from being used directly for filters with a large dynamic range, can be suppressed by the so-called degeneration resistance R_E in series with the emitter (see Fig. 4-7 (d)). The negative feedback will cause a decrease in the original transconductance g_m to the value

$$g'_m = \frac{g_m}{1 + g_m R_E} \approx \frac{1}{R_E} \text{ for } g_m \gg \frac{1}{R_E} \quad (4-6)$$

and in addition, a considerable linearization of the OTA and an increased swing of the input voltage. The S-T drawback consists in the fact that it can be used only as single-input single-

output OTA whereas the differential variants are more suitable for economical implementation of floating inductors. That is why more active elements must be used in a concrete filter than in the case of differential types of OTA, e.g. MAX435. The internal OTA in OPA615 and SHC615 has a differential input, but it cannot be used for linear applications because of its strongly nonlinear characteristic $I_{out} = f(V_{in})$. In addition, unlike with the S-T, a simple linearization technique does not exist here. Concrete experiments lead to the observation that the OPA860 is a useful element for active filters for the frequency range of units and tens of megahertz. A detailed description of the OPA860 parameters is given in [64]. A method for the simulation of floating inductor by S-T and voltage buffer is described below. Some parameters of 5th order video filter with an extremely flat group delay, which has been constructed on the basis of such synthetic inductors, are demonstrated.

4.2.1. Floating inductor replacement via “super-transistors”

The proposed circuit for inductance simulation with three S-T and one voltage buffer is given in Fig. 4-8. The schematic symbol of S-T also includes a possible degeneration resistor R_E for modifying the transconductance according to Eq. (4-7).

T_1 together with the voltage buffer acts as differential input OTA. Its output current I_1 is directly proportional to the transconductance g_{m1} of S-T No. 1:

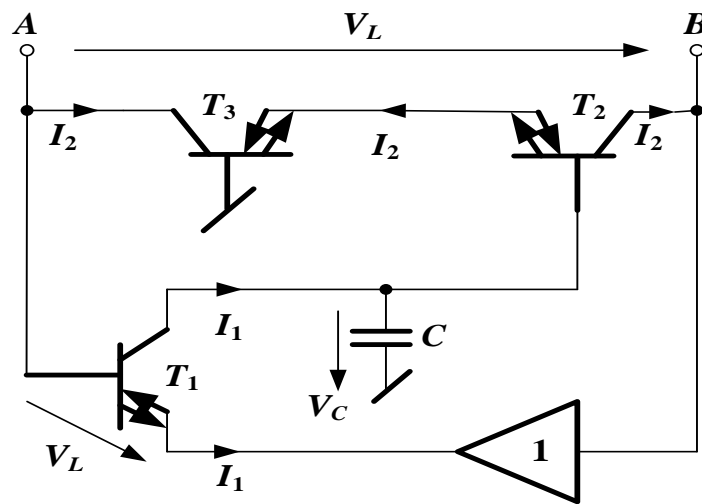


Fig. 4-8: Simulation of floating inductor.

$$I_1 = g_{m1} V_L \quad (4-7)$$

This current flows through the capacitor C and causes the voltage drop

$$V_c = \frac{I_1}{sC} = \frac{g_{m1}}{sC} V_L \quad (4-8)$$

Taking S-T with transconductance g_m as an ideal current conveyor CCII with a parasitic resistance $R_x = 1/g_m$ connected to its x terminal (i.e. to the emitter of S-T), then S-T No. 2 and 3 with interconnected emitters in Fig. 4-8, each with transconductances g_{m2} and g_{m3} , can be modeled as a connection of the ideal CCII (in place of T_3) and T_2 with its emitter connected to the parasitic resistance

$$R_x = \frac{1}{g_{m2}} + \frac{1}{g_{m3}} \quad (4-9)$$

The ideal T_3 provides zero voltage at its emitter and the current of T_2 is thus controlled only by the voltage across the capacitor. Its value is as follows:

$$I_2 = \frac{V_c}{R_x} = \frac{g_{m1}}{sCR_x} V_L \quad (4-10)$$

T_3 accomplishes the inversion of this current regardless of the real value of g_{m3} . That is why the circuit in Fig. 5-8 represents the lossless floating inductor with the inductance

$$L = C \frac{R_x}{g_{m1}} = \frac{C}{g_{m1}} \left(\frac{1}{g_{m2}} + \frac{1}{g_{m3}} \right) \quad (4-11)$$

A practical utilization of the proposed circuit has been verified on the example of 5th – order LC ladder video filter. All inductors of this filter were replaced by the synthetic inductors from Fig. 4-8. The frequency responses of the resulting active filter were measured and compared with the theoretical responses of passive LC prototype. These experiments are described in Section 4.2.3. This is preceded by an analysis of real influences of circuit components on the small-signal behavior of the filter as given in 4.2.2.

4.2.2. Real properties of synthetic inductor

The synthetic inductor in Fig. 4-8 is a two-terminal device whose small-signal frequency dependent behavior is affected by a number of factors, particularly by:

- Input resistance R_B and input capacitance C_B of terminal B (base) of S-T.
- Input resistance R_C and input capacitance C_C of terminal C (collector) of S-T.
- Transconductance of S-T, which can be modeled by a resistor R_x in series with the E terminal (emitter). The resistor R_x can also include the external degeneration resistor.
- Input resistance R_{buf} and input capacitance C_{buf} of the voltage buffer.
- Output resistance R_{Obuf} of the voltage buffer.

Assume that both building blocks of the synthetic inductor, i.e. S-T and buffer, are designed with the bandwidth required for the given application. Other real phenomena, e.g. frequency dependence of the buffer gain, parasitic inductance of the E-terminal of S-T, and others which affect the inductor parameters at relatively high frequencies, will not be included in the analysis.

The following parameters are mentioned in [64] for the OPA860 integrated circuit:

$$R_B = 455\text{k}\Omega, C_B = 2.1\text{pF}, R_C = 54\text{k}\Omega, C_C = 2\text{pF}, R_{buf} = 1\text{M}\Omega, C_{buf} = 2.1\text{pF}, R_{Obuf} = 1.4\Omega.$$

An analysis of circuit in Fig. 4-8 discloses the following consequences of the action of parasitic elements for the model of synthetic inductor:

Parasitic shunt resistance R_{A0} and capacitance C_{A0} act across the A terminal and the ground. R_{A0} or C_{A0} is given by a parallel combination of the resistance R_C or capacitance C_C of S-T No. 3 and the resistance R_B or capacitance C_B of S-T No. 1:

$$R_{A0} = R_{C1} \& R_{B1} \approx 48.3\text{k}\Omega, C_{A0} = C_{C3} + C_{B1} \approx 4.1\text{pF}.$$

Accordingly, the parasitic shunt resistance R_{B0} and capacitance C_{B0} act across the B terminal and the ground, where $R_{B0} = R_{C2} \& R_{buf} \approx 51.2\text{k}\Omega, C_{B0} = C_{C2} + C_{buf} \approx 4.1\text{pF}.$

The parasitic capacitances should be taken into account when designing the working capacitances of the LC ladder filter, which are connected to them in parallel. The parasitic resistances introduce additional losses into the circuit with possible degradation of the frequency response.

When designing the capacitance C inside the synthetic inductor, one should take into account the additional parasitic elements which are connected in parallel to this capacitor:

$$C_{cap} = C_{C1} + C_{B2} \approx 4.1\text{pF}, R_{cap} = R_{C1} \& R_{B2} \approx 48.3\text{k}\Omega.$$

Then the working capacitance should be decreased by C_{cap} . A symbolic analysis of the circuit in Fig. 4-8 leads to the formula for the impedance between terminals A and B :

$$Z_{AB} = \frac{R_{x1}(R_{x2} + R_{x3})}{R_{cap}} + sR_{x1}(R_{x2} + R_{x3})(C + C_{cap}) \quad (4-12)$$

Note that due to the finite parasitic resistance R_{cap} , the synthetic inductor has a lossy resistance R_s

$$R_s = \frac{R_{x1}(R_{x2} + R_{x3})}{R_{cap}} \quad (4-13)$$

A comparison of the second component on the right side of Eq. 4-12 and Eq. 4-13 confirms the conclusion that the value of the simulated inductance is modified by the capacitance C_{cap} , which is added to the working capacitance C .

The influence of the nonzero output resistance of the voltage buffer is the last effect examined. This resistance should be added to the resistance R_{x1} of S-T No. 1 in equations 4-12 and 4-13.

The above real properties are summarized in the model of the inductor in Fig. 4-9.

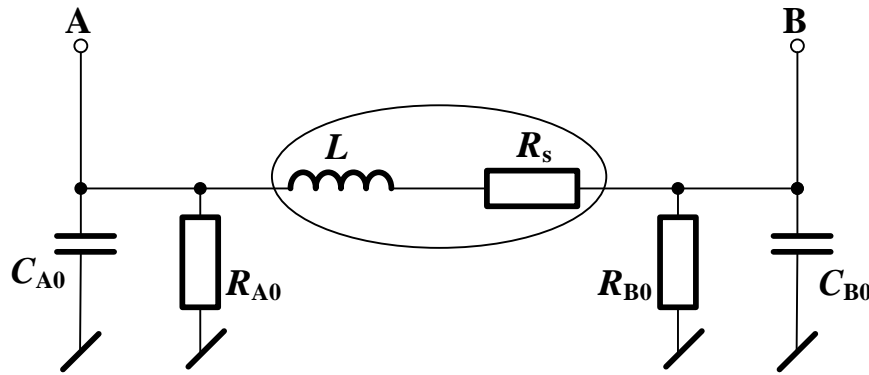


Fig. 4-9: Model of the synthetic inductor in Fig. 5-8, with the real effects considered.

4.2.3. Utilizing synthetic inductors for LC ladder simulation

Consider the realization of a lowpass LC ladder in Fig. 4-10. This filter has been designed on the basis of the following specification:

DC gain 0dB, cutoff frequency 5MHz, passband ripple 1dB, attenuation at least 50dB for frequencies above 27MHz, group delay ripple up to 3.58MHz less than 10ns. This specification corresponds to the parameters of commercial video filter FMS6400-1 by Fairchild Semiconductor [58].

The LC ladder has been designed according to the Feistel-Unbehauen approximation that is to say with the group delay response being maximally flat within the filter passband.

The active simulation of the filter from Fig. 4-10 by means of “super-transistors” is given in Fig. 4-11. T_{in} is designed with a high transconductance in order to provide low driving point impedance for the current source I_{in} . On the contrary, the transconductance of T_{out} is

lowered by a degeneration emitter resistor because T_{out} should act as a 100Ω load for the capacitor C_3 . Simultaneously this transistor provides an output current into a general load R_{out} .

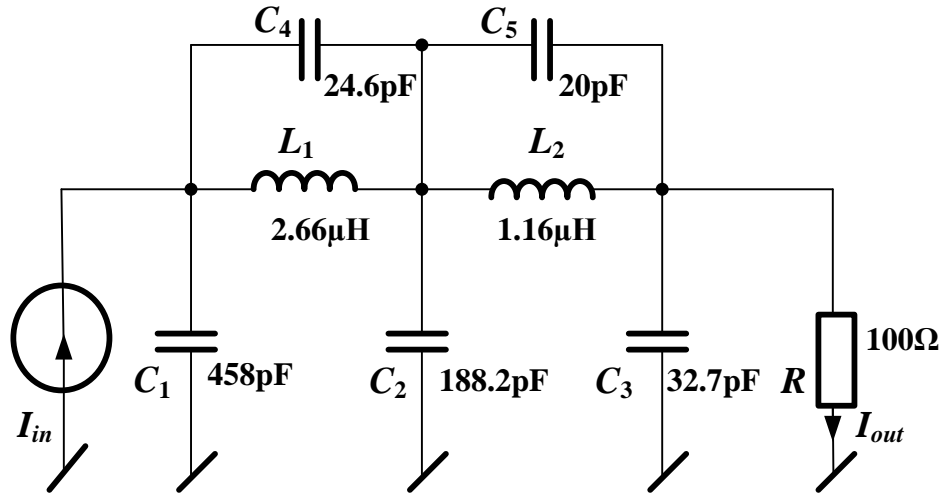


Fig. 4-10: 5MHz LC ladder filter.

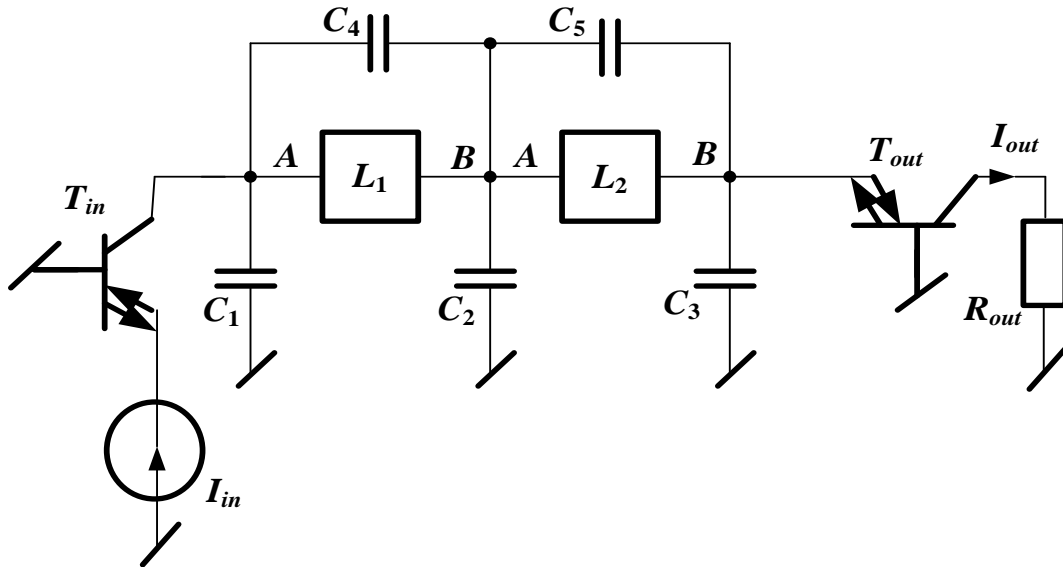


Fig. 4-11: Active implementation of the filter from Fig. 5-10. Blocks „L1“ and „L2“ are synthetic inductors from Fig. 4-8.

All the transconductance in the filter were implemented by the OPA860 integrated circuits. The S-T internal transconductance is set by an outside resistor R_Q , which is connected between the „ I_Q Adjust“ terminal and the negative supply voltage [58]. For the zero value of R_Q , the quiescent current is limited by an internal resistor, and the corresponding maximum g_m is approximately 95mA/V. This setting has been used for testing the filter. According to the datasheet recommendation, 100-Ohm series resistors were added to the base terminals of each S-T. “Super-transistors” were also complemented with 100-Ohm degeneration emitter

resistors, excepting T_{in} and T_{out} . For T_{in} , the emitter resistor was omitted in order to set $g_m = 95\text{mA/V}$. Then the input resistance of the filter is only 10.5Ω . The degeneration resistance for T_{out} is designed to be 89.5Ω . Taking into account the internal T_{out} transconductance, the total load resistance for C_3 is 100Ω .

The synthetic inductors in Fig. 4-8 were designed with $100\text{-}\Omega$ degeneration resistors for transistors T_1 and T_2 . The influence of the output resistance of the voltage buffer was neglected. The internal capacitors for inductors L_1 and L_2 were designed from Eq. 5-11 to be 199 pF and 87 pF , respectively. After subtracting the value of parasitic capacitance $C_{cap} = 4.1\text{ pF}$, the final values of working capacitances in the synthetic inductors are 195 pF and 83 pF . The capacitances C_1 , C_2 , and C_3 of the LC ladder in Fig. 4-11 were decreased by the parasitic capacitances C_{A0} , C_{B0} , and collector capacitance of T_{in} , specifically to values 452 pF , 180 pF , and 29 pF .

In Fig. 4-12, the frequency responses of active filter are compared with the ideal characteristics of LC ladder, analyzed in PSpice.

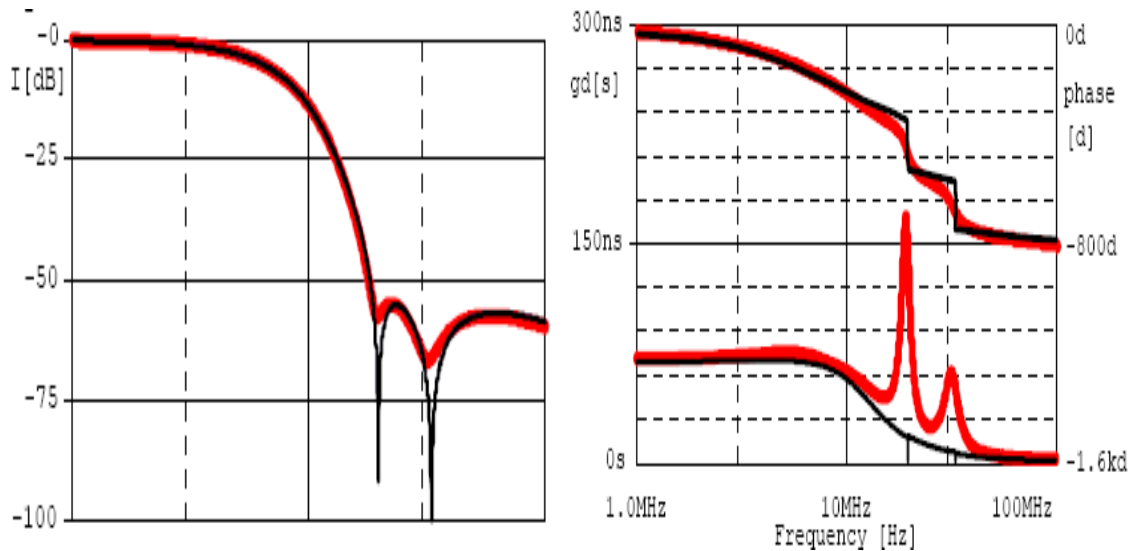


Fig. 4-12: Frequency responses of the active filter from Fig. 4-11. — ideal filter, — filter employing OPA860.

The amplitude frequency responses are in a good conformity. The plain stopband rejections are due to the finite values of quality factors of synthetic inductors (see Eq. 4-12). From the same reason, the phase response at these frequencies does not embody jump changes but its slope is adequately increased. That is why the group delay response shows significant peaks near the frequencies of transfer zeros. Fortunately, they occur in the filter stopband. The pass band group delay is 68 ns with a ripple of only 4 ns .

4.3. Floating GIC and its implementation

A novel Generalized Impedance Converter (GIC) is described in this section. The circuit consists of a pair of 2nd generation current conveyors and one voltage follower. A floating impedance Z_1 and two grounded impedances Z_2 and Z_3 are transformed into the input impedance according to the formula $Z_{in} = Z_1 * Z_3 / Z_2$. The circuit principle is verified via computer simulation.

4.3.1. Introduction

Impedance converters find application particularly in active filters, where they simulate circuit elements which are hard to integrate on a chip (especially inductors), or which must be set up artificially (e.g. Frequency Dependent Negative Resistors – FDNRs).

A study of the existing publications about impedance converters, e.g. [51], [65] and the papers referenced herein, leads to the conclusions summarized below:

A Generalized Impedance Converter (GIC) consists of NA active circuit elements and NP passive impedances Z_k , $k = 1, 2, \dots, NP$, where NP is (with only a few exceptions) an odd number. The input impedance of the converter is given as follows:

$$Z_{in} = \pm \frac{Z_1 Z_3}{Z_2 Z_4} \dots \frac{Z_{NP-2}}{Z_{NP-1}} Z_{NP} \quad (4-14)$$

The positive/negative sign in Eq. (5-14) appertains to the positive/negative impedance converter. The input terminals, between which the impedance is measured, can be either floating or one of them is grounded.

Such devices are frequently used to simulate inductors (one of the impedances in the denominator is of capacitive character), floating capacitors based on grounded capacitors (one of the impedances in the numerator is of capacitive character), FDNRs (two impedances in the numerator are of capacitive character), or the so-called high-order immittance (more impedances in the numerator/denominator have a capacitive character). Then the minimum possible number of passive elements NP is 3, 1, or 3 in the first, second and third case, respectively.

Formerly utilized operational amplifiers (Op Amps) are currently replaced by other active elements. One reason is the fact that in some cases the Op Amp-based impedance converters have a rather complicated topology and that their operation is based on fulfilling several relations among the parameters of passive elements. From this point of view, current

conveyors, particularly CCII+ or CCII-, appear to be more advantageous active elements for implementing the impedance converters [65].

In addition to the right-side impedances in Eq. (4-14), the ubiquitous parasitic impedances impact the circuit behavior and modify the equation for the input impedance. The results of the analysis of such modifications are often critical in selecting such circuit implementations of impedance converters which are suitable for a concrete application.

The work deals with a positive impedance converter with floating input terminals and with $NP=3$, which is potentially useful for the simulation of floating and grounded inductors, capacitors, and FDNRs. In [65], such converters are described which employ four CCII+ or CCII- and three impedances. An economical circuit employing only two current conveyors is given in [66]. However, this circuit requires several external passive elements and their parameters must fulfill exact matching conditions. The sensitivities of the input impedance to the parameters of these elements are then high. An interesting low-sensitive impedance converter with a pair of CCII- and $NP=5$ is proposed in [67] with the input impedance according to Eq. (4-14).

In this part, a novel implementation of floating positive impedance converter is described. It consists of three impedances, one CCII+, one CCII±, and one voltage buffer. The choice of such active elements was partially motivated by their easy implementation using commercially integrated circuits. Active elements such as CCII+ and buffer are directly available as OPA860 [64]. The CCII- can be compiled from two CCII+ [65].

4.3.2. Proposed impedance converter

The proposed impedance converter is shown in Fig. 4-13 (a).

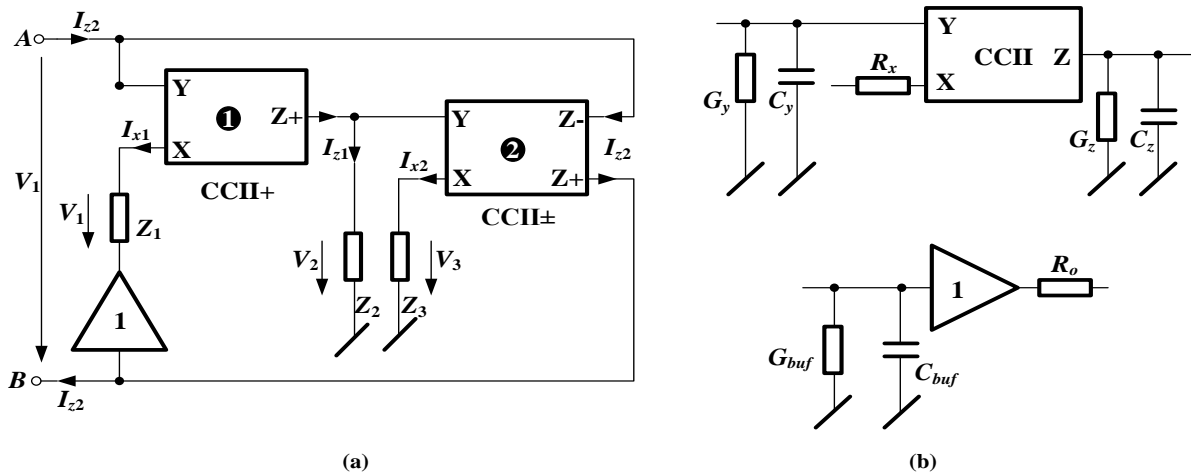


Fig. 4-13: (a) Proposed impedance converter, (b) Parasitic impedances of active element.

In the first step, let us assume that active elements of the converter are ideal. Then voltage V_1 between the A - B terminals appears at the impedance Z_1 and affects current $I_{x1} = V_1/Z_1$. This current also flows out of the $z+$ outlet as I_{z+} , causing a voltage drop at Z_2 , namely $V_2 = Z_2 I_{z1} = V_1 Z_2/Z_1$. This voltage is equal to voltage V_3 . Thus, the currents I_{x2} and I_{z2} are

$$I_{x2} = I_{z2} = \frac{V_3}{Z_3} = \frac{Z_2}{Z_1 Z_3} V_1$$

These currents are also the terminal currents. That is why the input impedance will be as follows:

$$Z_{in} = \frac{V_1}{I_{z2}} = \frac{Z_1}{Z_2} Z_3 = Z_1 Y_2 Z_3 \quad (4-15)$$

Comparing equations (4-15) and (4-14), one can conclude that in the ideal case, the circuit in Fig. 4-13 (a) behaves as a positive impedance converter with $NP = 3$.

4.3.3. Analysis of the influence of parasitic impedances

4.3.3.1. Alternative model of impedance converter

The dominant parasitic impedances of CCII and voltage buffer are shown in Fig. 4-13 (b): both the buffer input impedance and the impedance of y and z terminals of the conveyor are of capacitive character. In the low-frequency region, the output impedances of the buffer and the x terminal of the conveyor are resistive. When the frequency increases above a certain limit, which is given by the active device parameters, the inductive part of the impedance appears. Simple modeling in Fig. 4-13 (b) is accurate enough within a frequency band of up to circa tens or hundreds of MHz. Let us suppose that no other influences, such as frequency dependence of the buffer gain, will play a role in the working frequency region.

Specifically, the following parasitic parameters are mentioned in [64] for the OPA860 integrated circuit:

$$\begin{aligned} R_y = 455\text{k}\Omega &\Rightarrow G_y = 2.2\mu\text{S}, C_y = 2.1\text{pF}, R_z = 54\text{k}\Omega \Rightarrow G_z = 18.5\mu\text{S}, C_z = 2\text{pF} \\ R_{buf} = 1\text{M}\Omega &\Rightarrow G_{buf} = 1\mu\text{S}, C_{buf} = 2.1\text{pF}, R_o = 1.4\text{k}\Omega, R_x \geq 10.5\Omega \end{aligned} \quad (4-16)$$

The last specification is based on the fact that resistance R_x is inversely proportional to transconductance g_m , which can be adjusted electronically for OPA860. The highest value of g_m is approximately 95mA/V [64], which corresponds to the lowest value of R_x given above.

An analysis of the circuit in Fig 4-13 (a) shows the following consequences of the influence of parasitic elements Eq. (4-16) on the model of impedance converter:

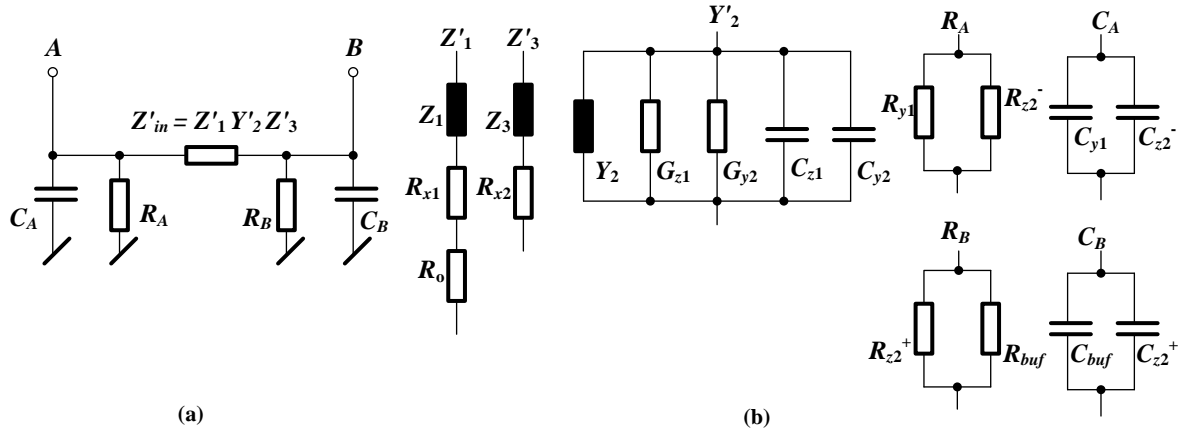


Fig. 4-14: Model of the impedance converter from Fig. 4-13, with real effects taken into consideration. The black impedances in (b) are working, the remaining are parasitic.

Parasitic shunt resistance R_A (R_B) and parasitic shunt capacitance C_A (C_B) act between the A (B) terminals and the ground. The parameters R_A , C_A , R_B , and C_B depend on the parasitic impedances of active elements according to Fig. 4-14 (b). Considering the nominal values for OPA860 according to Eq. (4-16), we get

$$\begin{aligned} R_A = R_{y1} \text{ \& } R_{z2-} &\approx 48.3\text{k}\Omega, & C_A = C_{y1} + C_{z2-} &\approx 4.1\text{pF} \\ R_B = R_{z2+} \text{ \& } R_{buf} &\approx 51.2\text{k}\Omega, & C_B = C_{buf} + C_{z2+} &\approx 4.1\text{pF} \end{aligned} \quad (4-17)$$

Such parasitic values should be taken into account when designing concrete applications of the impedance converter.

For the impedance between the A - B terminals, formula Eq. (4-15) is still true, but individual impedances on the right-side of the equation are modified by the parasitic impedances according to Fig. 4-14 (b). An analysis of these modifications is provided in the next sections for three concrete types of application of the impedance converter.

4.3.3.2. Simulation of floating inductor

The impedance converter will simulate the floating inductor on the following assumptions:

$$Z_1 = R_1, Y_2 = sC_2, Z_3 = R_3 \quad (4-18)$$

Eq. (4-15) then leads to the result

$$Z_{in} = sL, \quad L = R_1 R_3 C_2 \quad (4-19)$$

The parasitic impedances (see Fig. 4-14) will modify the input impedance as follows:

$$Z'_{in} = Z'_1 Y'_2 Z'_3 = (R_1 + R_{x1} + R_o)(sC_2 + G_{z1} + G_{y2} + sC_{z1} + sC_{y2})(R_3 + R_{x2})$$

After a small arrangement we get

$$Z_{in} = R' + sL' \quad (4-20)$$

Where

$$\begin{aligned} R' &= (R_1 + R_{x1} + R_o)(R_3 + R_{x2})(G_{z1} + G_{y2}), \\ L' &= (R_1 + R_{x1} + R_o)(R_3 + R_{x2})(C + C_{z1} + C_{y2}) \end{aligned} \quad (4-21)$$

The parasitic impedances cause a modification of simulated inductance. In addition, a series lossy resistance R' appears. The ratio of the imaginary to the real part of impedance in Eq. (4-20) is

$$\frac{\omega L'}{R'} = \omega \frac{C + C_{z1} + C_{y2}}{G_{z1} + G_{y2}} \quad (4-22)$$

Ratio of Eq. (4-22) is the inductor quality factor, or the reciprocal value of the $\tan(\delta)$ at the frequency ω . To maximize it during the inductor design while simultaneously respecting concrete parasitic impedances, we should maximize the working capacitance C_2 and minimize the resistances R_1 and R_3 . From this point of view, the working resistors should be designed as short circuits. Then the parasitic resistances would substitute their role. This seems to be unpractical due to the direct dependence of the simulated inductance on the parasitic elements. However, an interesting possibility appears when using integrated circuits such as OPA860, where the resistance of the x terminal can be electronically set to a defined value.

Then the above conditions $R_1 = 0$, $R_3 = 0$ can be used for a consistent optimization.

4.3.3.3. Simulation of floating capacitor

The simulation of the floating capacitor whose capacitance is derived from the capacitance of another grounded capacitor is feasible on the assumption that

$$Z_1 = R_1, Y_2 = \frac{1}{R_2}, Z_3 = \frac{1}{sC_3} \quad (4-23)$$

Then

$$Z_{in} = \frac{1}{sC}, \quad C = C_3 \frac{R_2}{R_1} \quad (4-24)$$

Considering the influence of the parasitic impedances according to Fig. 4-14 (b), we obtain modified input impedance

$$Z'_{in} = R' + sL' + \frac{1}{sC'} \quad (4-25)$$

Where

$$\begin{aligned} R' &= (R_1 + R_{x1} + R_o) \left[\frac{C_{z1} + C_{y2}}{C_3} + R_{x2}(G_2 + G_{y1} + G_{y2}) \right], \\ L' &= (R_1 + R_{x1} + R_o)R_{x2}(C_{z1} + C_{y2}), \\ C' &= \frac{C_3}{(R_1 + R_{x1} + R_o)(G_2 + G_{z1} + G_{y2})} \end{aligned} \quad (4-26)$$

Note that a parasitic resistor and a parasitic inductor appear in series with the simulated capacitor. A simple computation reveals the values of resonant frequency ω_r and quality factor Q of the corresponding series resonance tank:

$$\omega_r = \sqrt{\frac{G_2 + G_{z1} + G_{y2}}{R_{x2}C_3(C_{z1} + C_{y2})}}, \quad Q = \frac{\sqrt{\alpha}}{1 + \alpha} \quad (4-27)$$

Where

$$\alpha = \frac{C_{z1} + C_{y2}}{R_{x2}C_3(G_2 + G_{z1} + G_{y2})} \quad (4-28)$$

An analysis shows that the quality factor cannot be greater than 0.5 in any case. In other words, the circuit is well damped. Throughout the converter design, the C_3 and G_2 parameters should be chosen such that they shift the resonant frequency sufficiently beyond the working frequency region of a given application.

4.3.3.4. Simulation of the FDNR

Theoretically, the ideal FDNR can be simulated using the impedance converter in Fig. 4-13 (a) under the following conditions:

$$Z_1 = \frac{1}{sC_1}, \quad Y_2 = \frac{1}{R_2}, \quad Z_3 = \frac{1}{sC_3} \quad (4-29)$$

Then

$$Z_{in} = \frac{1}{s^2 D}, \quad D = R_2 C_1 C_3 \quad (4-30)$$

The influence of the parasitic impedances causes the modified result

$$Z'_{in} = R' + sL' + \frac{1}{sC'} + \frac{1}{s^2D'} \quad (4-31)$$

Where

$$\begin{aligned} R' &= (C_{z1} + C_{y2}) \left[\frac{R_{x1} + R_o}{C_3} + \frac{R_{x2}}{C_1} \right] + R_{x2}(R_{x1} + R_o)(G_2 + G_{z1} + G_{y2}), \\ L' &= (R_{x1} + R_o)R_{x2}(C_{z1} + C_{y2}), \\ \frac{1}{C'} &= \frac{C_{z1} + C_{y2}}{C_1 C_3} + (G_2 + G_{z1} + G_{y2}) \left[\frac{R_{x1} + R_o}{C_3} + \frac{R_{x2}}{C_1} \right], \\ D' &= \frac{C_1 C_3}{G_2 + G_{z1} + G_{y2}} \end{aligned} \quad (4-32)$$

In reality, the value of D is modified, and there also appears a lossy resonant circuit in series with the FDNR.

4.3.4. Design example

As an example, let us design a floating capacitor with $C = 10\text{nF}$ on the basis of a grounded capacitor with the capacitance $C_3 = 100\text{pF}$. The capacity must therefore be multiplied 100 times. A design rule $R_2 = 100R_1$ results from Eq. (4-24) which is true for an ideal case without any parasitic impedances of active elements being taken into consideration.

Consider current conveyors with the parameters of OPA860 circuits according to Eq. (4-16). The x -resistance of CCII No. 1 will be set to 98.6Ω . Together with the buffer output resistance R_o , it forms the resistance $R_1 = 100\Omega$. The resulting resistance will be weakly dependent on the value of parasitic resistance R_o . The resistance R_2 will be designed such that it creates, together with parasitic resistances R_{z1} and R_{y2} , a hundredfold of R_1 , i.e. $10\text{k}\Omega$. A simple calculation leads to the value $12.6\text{k}\Omega$. The resistance R_{x2} should be selected as small as possible, i.e. 10.5Ω , since it operates in series with the working capacitor and decreases its quality factor.

A computer simulation of the frequency dependence of the A - B impedance has been performed using the SNAP program [41] with the result given in Fig. 4-15. A curve for the ideal capacitor with $C=10\text{nF}$ is added for comparison. There is good agreement up to 2MHz .

Then the influence of the series resistance R' (see Eq. (4-25) or (4-26) shows up, and the parasitic inductance starts increasing the impedance from frequencies exceeding ca. 100MHz.

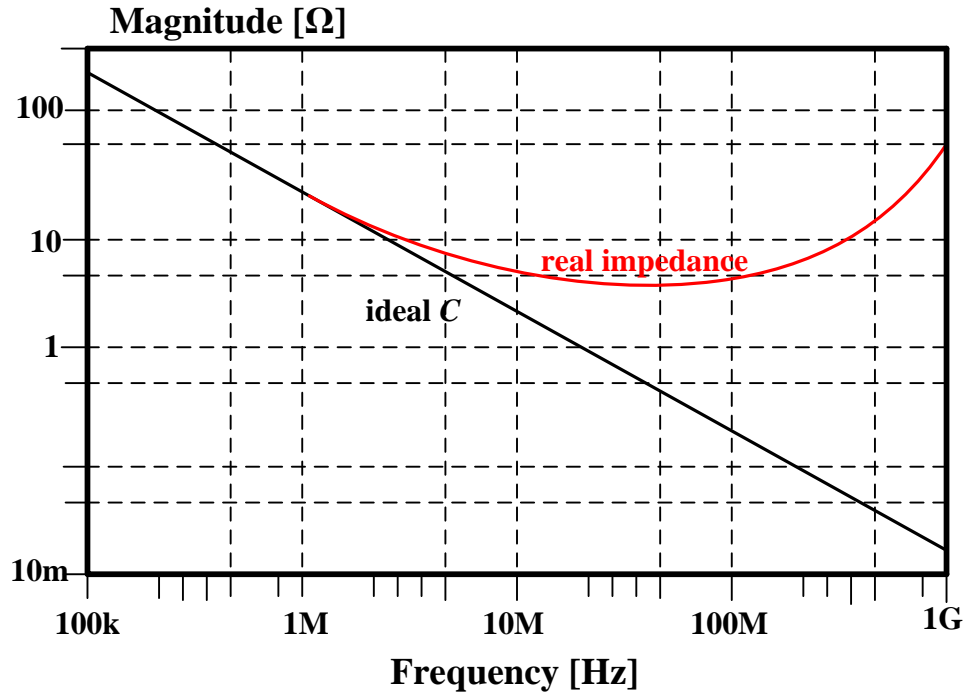


Fig. 4-15: Simulation of the frequency dependence of the impedance of the synthetic floating capacitor.

The positive impedance converter described has the following features: (i) Two current conveyors CCII and one voltage buffer are the only required active elements, (ii) two of three internal impedances are grounded, (iii) all the active elements are available as commercial integrated circuits. In addition, note that the negative impedance converter can be easily obtained from the positive one by merely interchanging the current outputs of the CCII No. 2. An impedance converter for simulating the grounded, not the floating impedance originates from the circuit either by grounding the A terminal and omitting the z - terminal of CCII No. 2, or by grounding the B terminal, omitting the $z+$ terminal of CCII No. 2, and replacing the buffer by a short circuit.

4.4. Voltage Differencing Transconductance Amplifier for Filter Implementation

Presently, there is the interest of the availability of building active filters and other signal processing circuits without the use of physical coils. Although, a spiral inductor can be realized in an integrated circuit, it still has some drawbacks in the usage of space, weight, cost and tunability.

The inductance simulators can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element. The attention is subsequently focused on the inductance simulation using different high-performance active building blocks such as, Operational Transconductance Amplifiers (OTAs) [58], current feedback op-amps [27], and four-terminal floating nullors (FTFNs) [60], current conveyors [61-64], current differencing buffered amplifier (CDBAs) [65], etc. The literature surveys shows that a large number of circuit realizations for floating and grounded inductance simulators have been reported [58], [65].

In this section, we present novel floating simulators employing Differencing Transconductance Amplifier (VDTA), which is proven to be quite useful in either current or voltage-mode signal processing circuits.

4.4.1. Synthetic inductor based on VDTA

Fig. 4-16 shows a synthetic floating inductor which employ one of Voltage Differencing Transconductance Amplifier (VDTA) which contains Differential Input Single Output OTA (DISO) and Single Input Differential Output OTA (SIDO), and one grounded capacitor C_L .

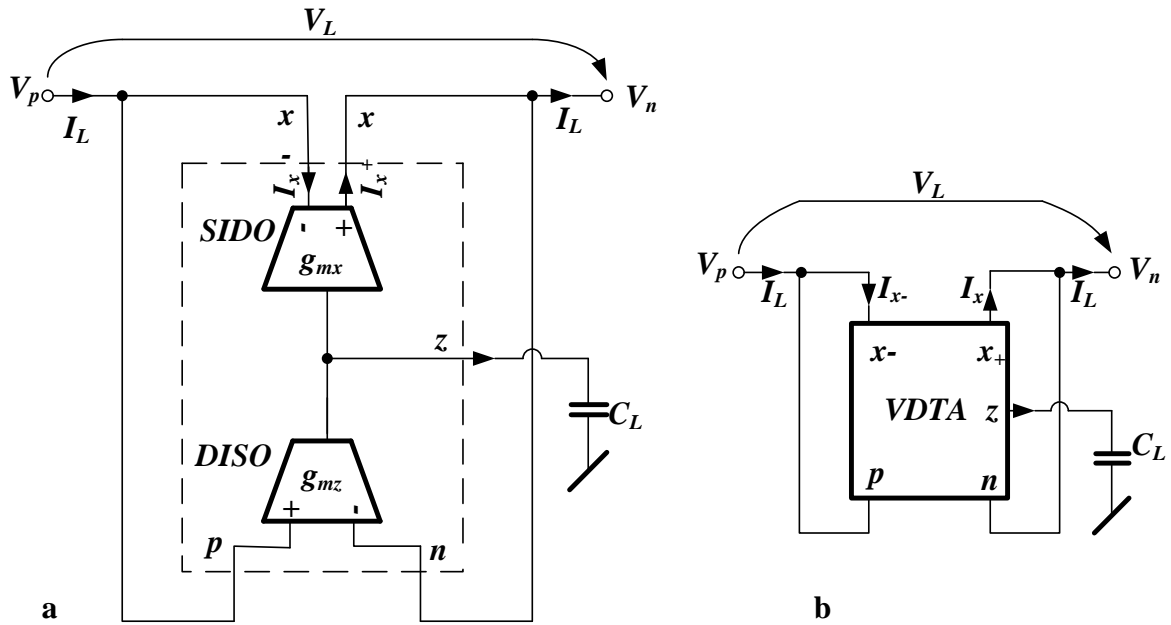


Fig. 4-16: (a) Synthetic inductor circuit employing DISO OTA and SIDO OTA, (b) simplified representation of the synthetic inductor by VDTA.

The process of transforming voltage difference ($V_P - V_n$) into current I_z of DISO OTA is described by the equation:

$$I_z = g_{mz}(V_p - V_n) \quad (4-33)$$

Current I_z causes voltage across the capacitor, and this voltage is transformed into current I_x .

$$V_c = \frac{I_z}{sC_L} = \frac{g_{mz}(V_p - V_n)}{sC_L} \quad (4-34)$$

$$I_x = g_{mx}V_c \quad (4-35)$$

$$I_x = g_{mx}g_{mz} \frac{(V_p - V_n)}{sC_L} \quad (4-36)$$

$$Z_{in} = \frac{I_x}{(V_p - V_n)} = \frac{g_{mx}g_{mz}}{sC_L} \quad (4-37)$$

The circuit, thus, simulates a floating inductor with the resulting inductance given by

$$L = \frac{g_{mx}g_{mz}}{C_L} \quad (4-38)$$

4.4.2. Low-pass LC Ladder simulation

Fig. 4-17 shows the schematic of a lowpass LC ladder filter which has been designed according to Caue approximation on the basis of the following specifications:

DC gain 0dB, 3-dB cutoff frequency 25kHz, ripple 2dB, 40dB for frequency above 55kHz, third-order.

The active simulation of the passive LC ladder filter from Fig. 4-17 by means of Voltage Differencing Transconductance Amplifier (VDTA) is given in Fig. 4-18.

The proposed floating inductor circuit in Fig. 4-16 is realized with the following values: $g_{mz} = g_{mx} = 96.8 \mu\text{S}$ with R_{adj} equal to $10\text{k}\Omega$ according to Table 3-5.

From equation (4-38)

$$C_L = L g_{mz}g_{mx} = 441\text{pF}$$

The VDTA is simulated by using the schematic implementation shown in Fig. 3-36 with DC power supply voltages equal to $V_{DD} = V_{SS} = \pm 0.6$ V. The simulations are performed by using CMOS structure and MIETEC 0.18 μ m CMOS process model technology parameters.

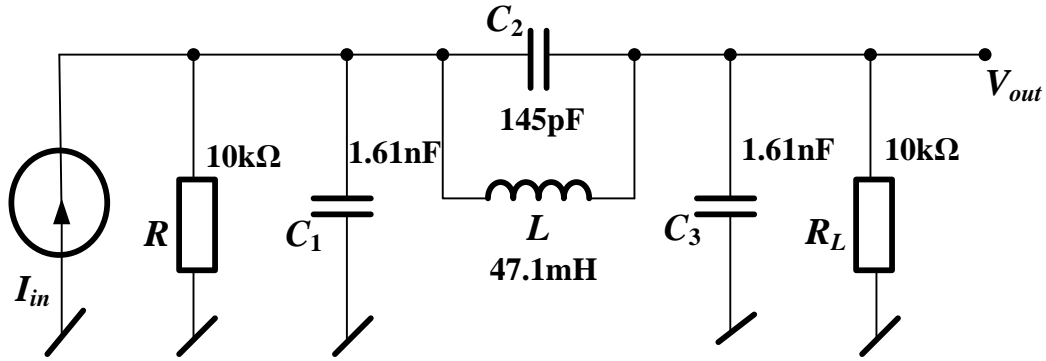


Fig. 4-17: 25kHz LC ladder filter.

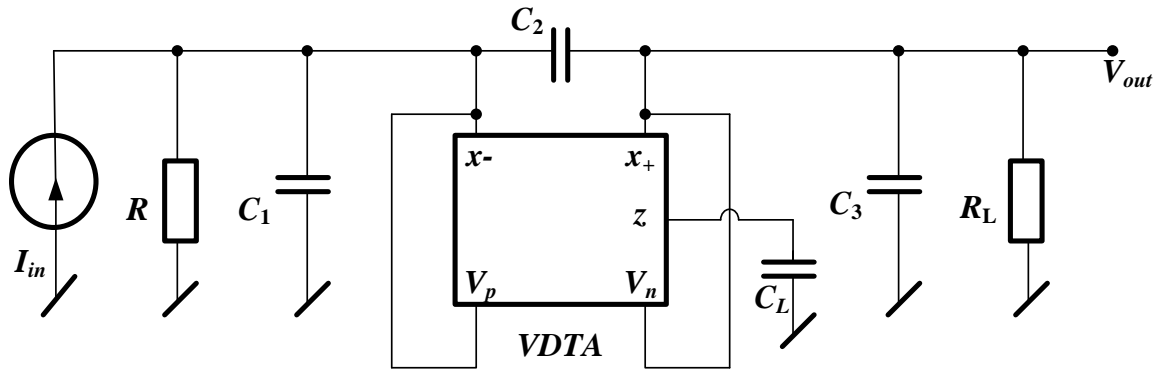


Fig. 4-18: Active implementation of the filter from Fig. 4-17.

The frequency responses and the group delay of the filter are shown in Figs. 4-19, and 4-20, respectively. It can be seen that the simulation using the true inductor and its VDTA simulators are in good agreement.

Fig. 4-21 shows that the magnitudes of the impedances of an ideal inductor with value equal to 47.1mH which we used in LC ladder filter in Fig. 4-17, and its simulator circuit by Voltage Differencing Transconductance Amplifier (VDTA) as shown in Fig. 4-18 with C_L equal to 441pF can be made very close for a set of selected values over many decades.

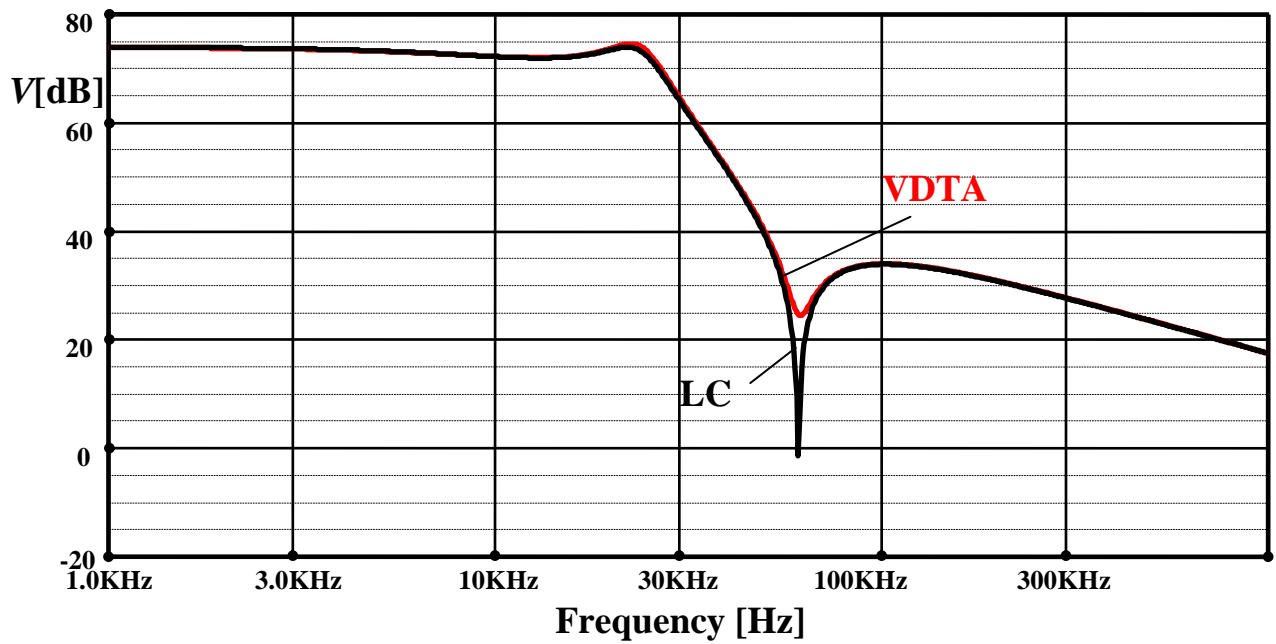


Fig. 4-19: The frequency responses of ideal LC ladder and VDTA-based active filter.

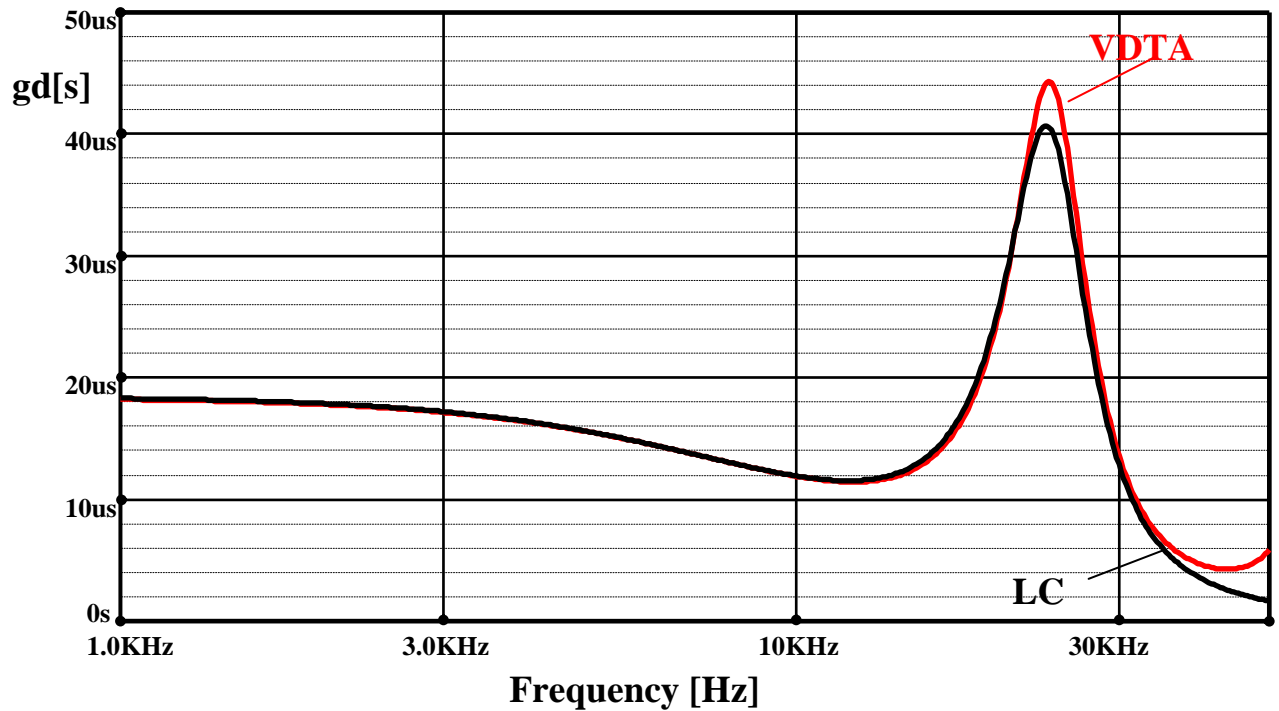


Fig. 4-20: The group delay response of ideal LC ladder and VDTA-based active filter.

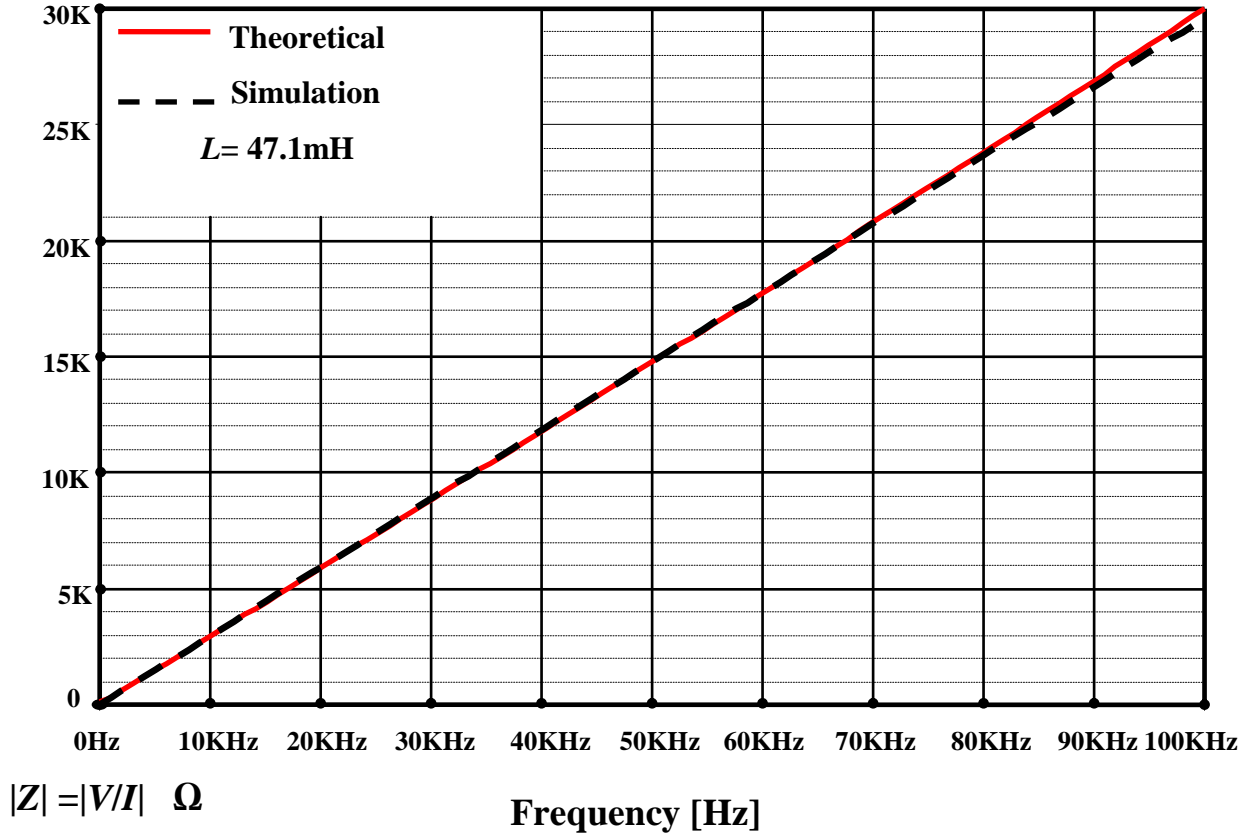


Fig. 4-21: The impedance values relative to frequency of the ideal and simulated inductors.

4.4.3. Band-pass LC Ladder simulation

Fig. 4-22 shows the schematic of 8th order a band-pass LC ladder filter which has been designed according to Cauer approximation on the basis of the following specifications:

8th order, central frequency = 10kHz, ripple 1dB, 60dB attenuation, $B_1 = 5\text{KHz}$, $B_2 = 20\text{KHz}$

The active simulation of the passive LC ladder filter from Fig. 4-22 by means of Voltage Differencing Transconductance Amplifier (VDTA) is given in Fig. 4-23.

The proposed floating inductor circuit in Fig. 4-22 is realized with the following values: $g_{mz} = g_{mx} = 96.8 \mu\text{S}$ with R_{adj} equal to $10\text{k}\Omega$ according to Table 3-5.

It follows from equation (4-38) that

$$\begin{aligned}
 C_{L1} &= L_1 g_{mz} g_{mx} = 3.85\text{nF}, & C_{L2} &= L_2 g_{mz} g_{mx} = 403.7\text{pF}, \\
 C_{L3} &= L_3 g_{mz} g_{mx} = 1.662\text{nF}, & C_{L4} &= L_4 g_{mz} g_{mx} = 6.375\text{nF} \\
 C_{L5} &= L_5 g_{mz} g_{mx} = 773.7\text{pF}
 \end{aligned}$$

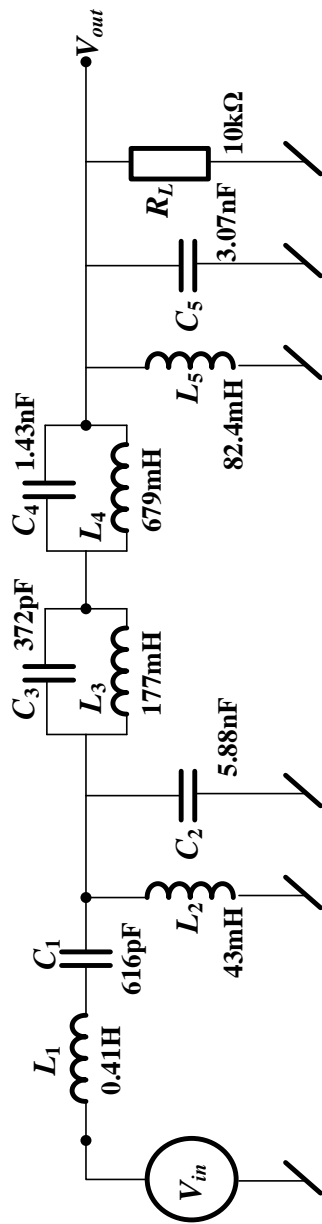


Fig. 4-22: Band-pass 8th order LC ladder filter.

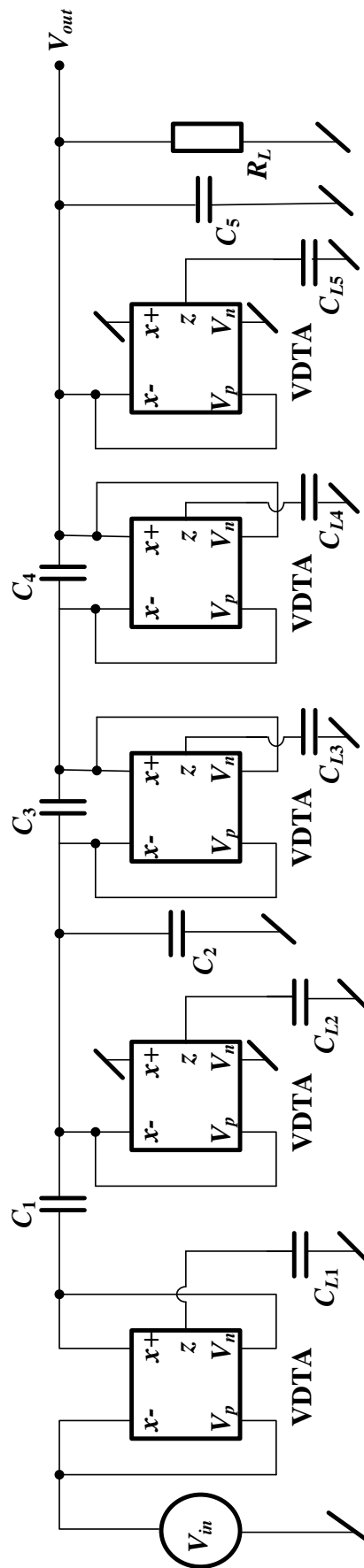


Fig. 4-23: Active implementation of the filter from Fig. 4-22.

The frequency responses of the filter are shown in Fig. 4-24. It can be seen that the simulation using the true inductor and its VDTA simulators are in good agreement.

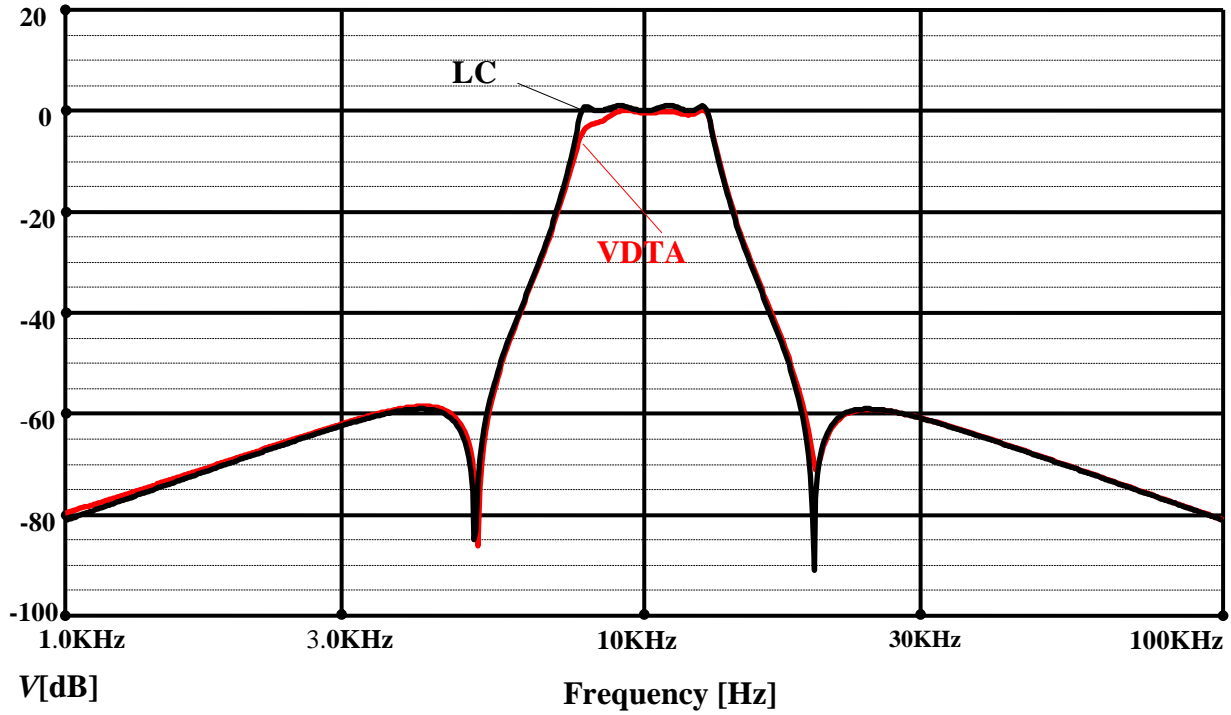


Fig. 4-24: The frequency responses of ideal LC ladder and VDTA-based active filter.

4.4.4. Design of resistor-less first-order all-pass filter using single VDVTA

All-pass filters (APFs) find applications where frequency dependence of phase, or phase linearity or group delay flatness can be major design consideration. They have been exhaustively investigated over the last decade or so. As far as first-order APFs are concerned, most of these circuits use several passive components [68–71]. On the other hand, recently proposed resistor less first-order AP filters [69] use two capacitors (one of them is floating) and suffer from the need of passive component ratio-matching conditions, as well as product performance variability problems because of their dependence on op-amp internal compensation capacitors.

In analog signal processing, first-order all-pass filters are widely used to shift the phase of the input signal from 0 to 180° or from 180° to 0 while keeping its amplitude constant over the desired range of frequency.

Fig. 4-25 and Fig. 4-26 illustrate proposed transimpedance -mode all-pass filters using two OTAs with high input and low output impedances and its implementation by single VDVTA and one grounded capacitor, respectively.

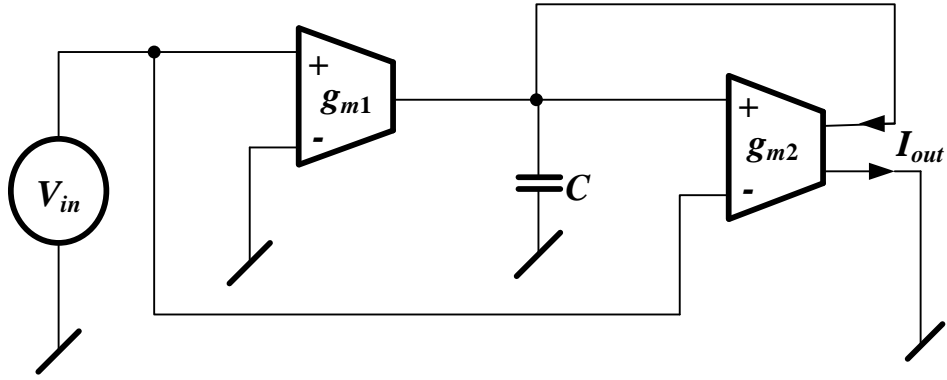


Fig. 4-25: The all-pass filter by OTAs.

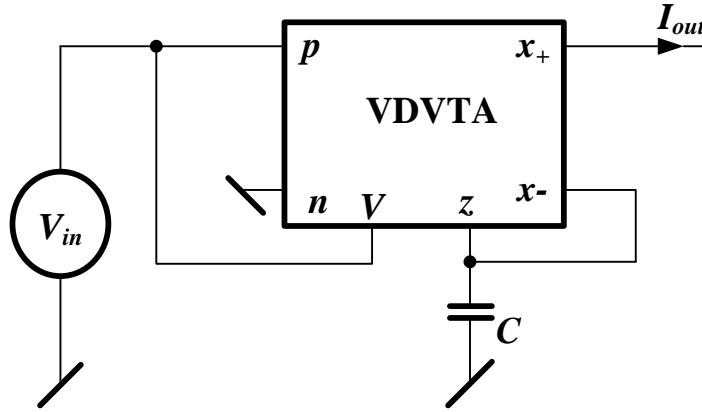


Fig. 4-26: Implementation of all-pass filter in Fig. 4-25 by using VDVTA.

The proposed circuits shown in Figs. 4-25 and 4-26 yield the following transimpedance transfer function:

$$\frac{I_{out}}{V_{in}} = \frac{g_{m1} - sC}{g_{m2} + sC} g_{m2} \quad (4-39)$$

The proposed APFs shown in Figs. 4-25 and 4-26 have been simulated using PSPICE. During these simulations, the CMOS-based structure of Fig. 3-38 has been used. The device model parameters are taken from TSMC 0.18 μ m CMOS process. The ± 0.6 V supply voltages all g_m equal to 96.8 μ S were used.

Figs. 4-27 and 4-28 show the magnitude and phase responses respectively for the all-pass filtering signal. The simulated results of all-pass filter by OTA obtained agree well with the VDVTA-based all-pass filter.

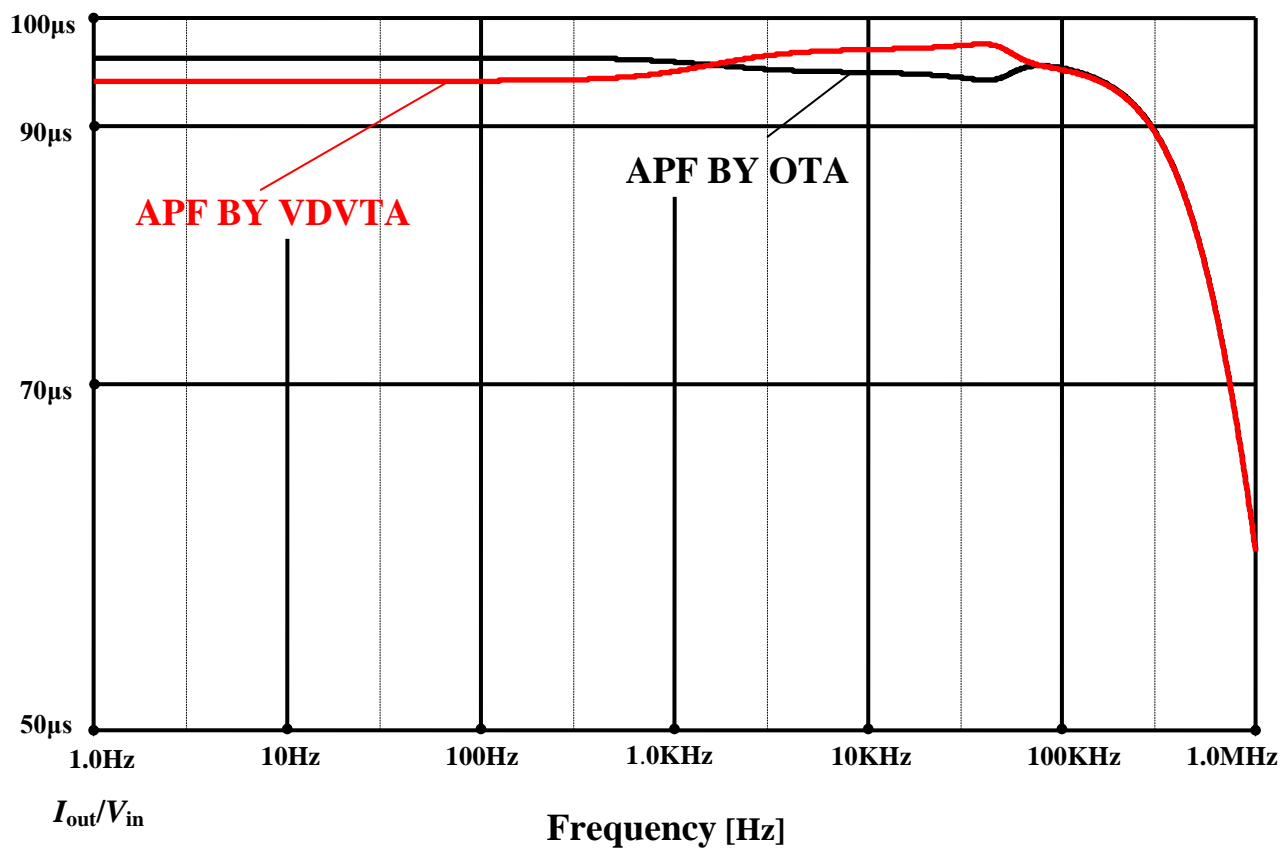


Fig. 4-27: Amplitude frequency responses of all-pass filters.

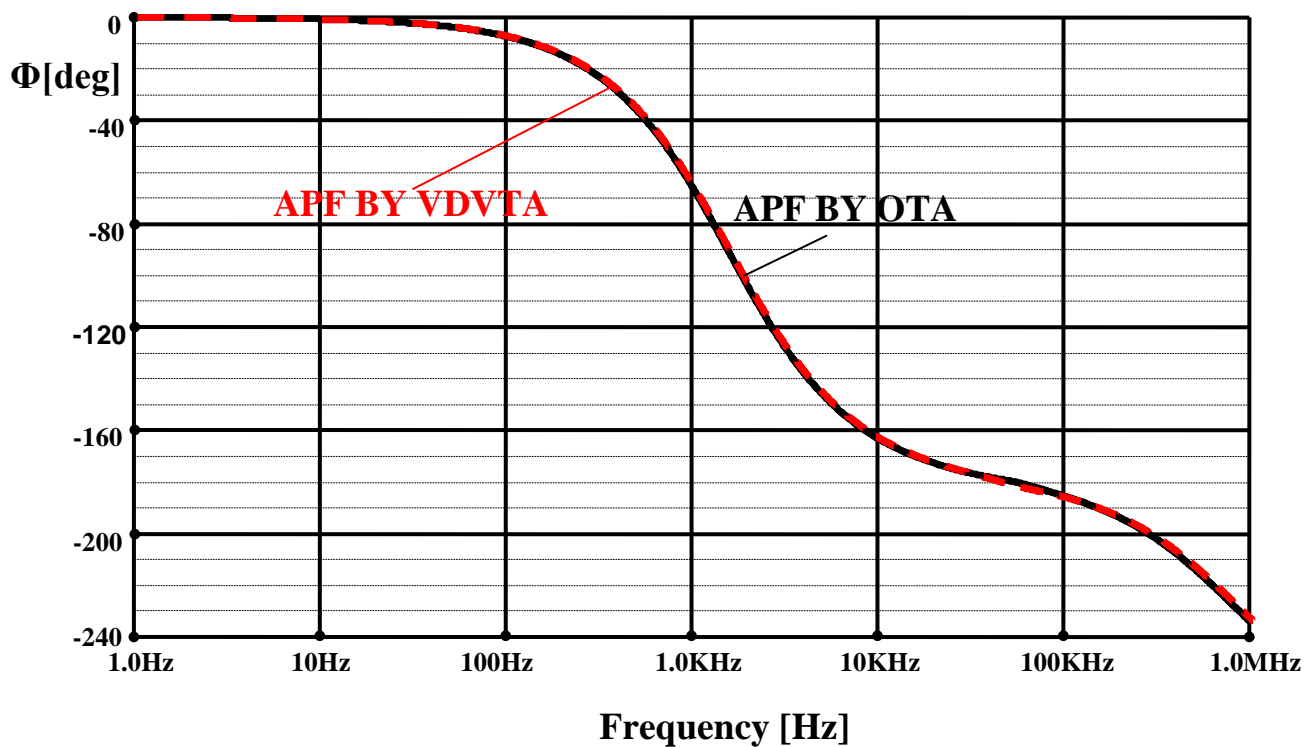


Fig. 4-28: Phase frequency responses of all-pass filters.

4.4.5. Design of KHN filter using VDTA

The Kerwin–Huelsman–Newcomb (KHN) biquad filter [72], [73] belongs to popular filter structures of the type of “two integrators in the feedback loop”. An important feature of this structure is the generation of all three basic filter transfer functions, i.e., low-pass (LP), band-pass (BP), and high-pass (HP) simultaneously.

The well-known voltage-mode 2nd-order KHN filter [72], [73] in Fig. 4-29 is preferred building block for cascade filter design. This circuitry can be understood as a single-input three-output device, generating three basic 2nd-order transfer functions (low-pass, band-pass, and high-pass).

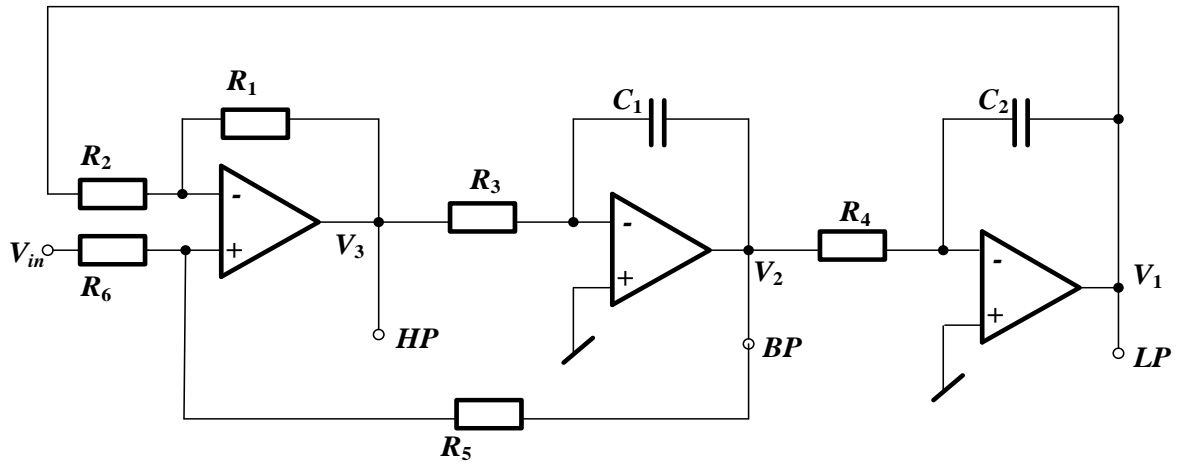


Fig. 4-29: Classical structure of the KHN filter.

In addition, as obvious from the flow-graph in Fig. 4-30, filter tuning without modifying the quality factor can be done by simultaneous modification of $R_3=R_4$. For identical values of R_1 , R_2 , R_5 and R_6 the DC gain of LP, high frequency gain of HP, and maximum gain of BP filters are fixed to their unity-values while tuning, and thus the upper bound of the filter dynamic range remains unchanged.

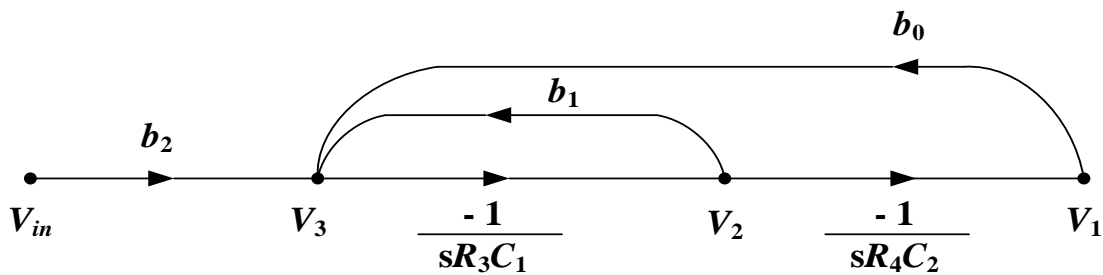


Fig. 4-30: The corresponding flow-graph of KHN in Fig. 4-29. For $R_1 = R_2 = R_5 = R_6$, $b_2 = b_1 = -b_0 = 1$.

Recently, many methods were published how to implement the KHN structure by means of active elements other than voltage Op Amps, in particular by current conveyors [74-76], but also by CDBA (Current-Differencing Buffered Amplifier) [77], [78] or DO-DDCC (Differential-Output Differential Difference Current Conveyor) elements [55].

In this part, the classical KHN structure is transformed into the current mode by utilizing the VDTA (Voltage Differencing Transconductance Amplifier) circuit elements [80], whose input and output signals are currents. The final filter consists of only two VDTAs and two grounded capacitors, and thus it can be classified as so-called VDTA-C filter, an analogy with the well-known gm-C filters.

A possible CMOS-based VDTA circuit realization suitable for the monolithic IC fabrication is displayed in Fig. 3-36. The proposed VDTA-based CM KHN biquad is given in Fig. 4-31.

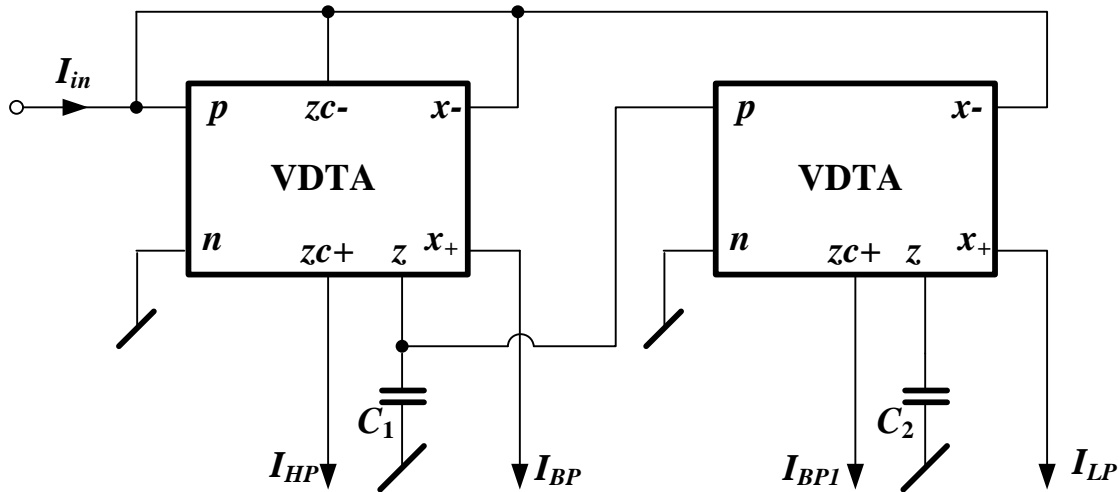


Fig. 4-31: VDTA-based CM KHN circuit.

The signal-flow graph in Fig. 4-30 can be redrawn for currents as shown in Fig. 4-32, together with the corresponding VDTA-based biquad. In contrast to conventional Op Amp, the VDTA enables an easy implementation of the non-inverting integrator. The non inverting integrators in the feedback loops require the signs of gains of the feedback branches to be modified, as follows from a comparison of the graphs in Figs. 4-32 and 4-30.

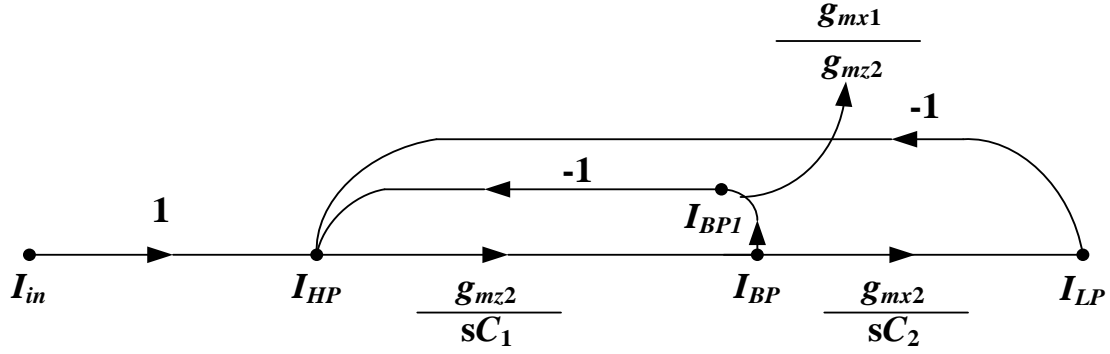


Fig. 4-32: The corresponding flow-graph of KHN in Fig. 4-31.

Evaluating the flow-graph in Fig. 4-32 yields the following transfer functions:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2}{s^2 + s \frac{g_{mx1}}{C_1} + \frac{g_{mz2}g_{mx2}}{C_1C_2}} \quad (4-40)$$

$$\frac{I_{BP}}{I_{in}} = \frac{s \left(\frac{g_{mz2}}{C_1} \right)}{s^2 + s \frac{g_{mx1}}{C_1} + \frac{g_{mz2}g_{mx2}}{C_1C_2}} \quad (4-41)$$

$$\frac{I_{BP1}}{I_{in}} = \frac{s \left(\frac{g_{mx1}}{C_1} \right)}{s^2 + s \frac{g_{mx1}}{C_1} + \frac{g_{mz2}g_{mx2}}{C_1C_2}} \quad (4-42)$$

$$\frac{I_{LP}}{I_{in}} = \frac{\frac{g_{mz2}g_{mx2}}{C_1C_2}}{s^2 + s \frac{g_{mx1}}{C_1} + \frac{g_{mz2}g_{mx2}}{C_1C_2}} \quad (4-43)$$

Where

$$\omega_0 = \sqrt{\frac{g_{mz2}g_{mx2}}{C_1C_2}}, \quad B = \frac{\omega_0}{Q} = \frac{g_{mx1}}{C_1} \quad (4-44)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \frac{\sqrt{g_{mz2}g_{mx2}}}{g_{mx1}} \quad (4-45)$$

It follows from Eqs (4-40), (4-41), (4-42), and (4-43) that the above filter structure in Fig. 4-31 provides basic highpass, lowpass, and bandpass operations. Due to current output signals, a simple implementation of other types of the transfer functions can be accomplished via a proper combination of these currents.

It follows from Eqs (4-44) and (4-45) that

- (a) the natural frequency ω_0 can be tuned via the transconductances g_{mz2} and/or g_{mx2} and/or via capacitance C_2 without disturbing the filter bandwidth B ,
- (b) the filter bandwidth B can be controlled independently of ω_0 via g_{mx1} ,
- (c) the quality factor Q can be controlled independently of ω_0 via g_{mx1} .

To verify the theoretical analysis, the CM KHN filter configuration presented in this study is simulated in SPICE circuit simulation program using the CMOS-based VDTA circuit given in Fig. 3-36. Here, 0.18 μm MIETEC real transistor model parameters are implemented for all transistors in the circuit. The symmetrical supply voltages of $\pm 0.6\text{V}$ were used. Fig. 4-33 demonstrates the results of CM KHN biquad circuit simulations when $C = C_1 = C_2 = 10 \text{ nF}$, $g_{mx1} = g_{mz1} = g_{mx2} = g_{mz2} = 96.82 \mu\text{S}$, which corresponds to the theoretical natural frequency of 1.57 kHz. The simulated value is 1.54 kHz. Therefore, the CMOS-level simulation confirms well the theoretical assumptions.

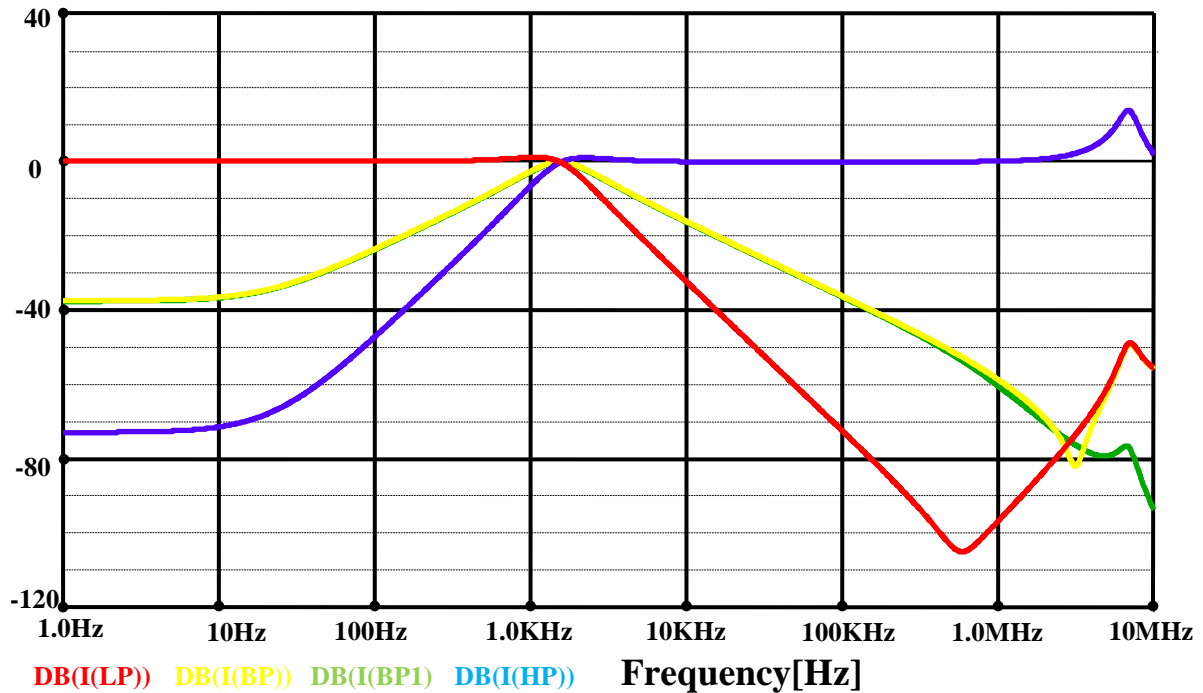


Fig. 4-33: Results of circuit simulations for CM KHN circuit using CMOS-based VDTAs.

5. Conclusion

In the last decade, for analogue signal processing huge number of active building blocks was introduced, however, there is still the need to develop new active elements that offer new and better advantages. Therefore, the main contribution of this thesis was the definition of such novel ABBs, and their application possibilities.

The theoretical and practical results of the work were presented in two main chapters, which introduced the novel introduced blocks and moreover proved the possibility of the implementation of these blocks.

The new high linearity, wideband bulk-driven OTA with tunable transconductance was designed. This OTA is then used for designing active building blocks (CDTA, VDTA, VDVTA, and DVCC).

In this thesis I presented some new active building blocks as (VDTA, and VDTVTA). As applications, several filters structures current-, voltage- and mixed-mode by using VDTA, and VDVTA was presented.

Novel structures of first-order all-pass filters based on VDVTA and novel structures of second-order universal filters, KHN-equivalent circuits by novel active element (VDTA) proposed in this thesis.

Thesis also was focused on LC ladder simulation on the principle of inductor replacement by synthetic inductor.

The floating inductor was synthesized via:

1. MAX435, a commercial OTA [57], [64], which appears to be an optimal circuit element for such designs. Its differential input and output can be utilized for the simplification of the well-known circuitry for simulating the floating inductor. The transconductance of MAX435 is adjusted by an external two-terminal device. In the case of linear resistor, OTA has an extremely linear I&V characteristic. The limitations of the output current can be precisely set by another external resistor.
2. „super-transistor“ (S-T), which is commercially available in several versions, e.g. OPA615, SHC615, OPA860, and OPA861 [64].
3. Newly introduced VDTA and VDVTA elements [55] designed in the first part of the thesis.

The presented work represents the investigation on building blocks for modern current-mode and mixed mode based integrated circuits. A number of novel introduced building

blocks together with their implementation are the results. The functionality of the proposed blocks was proved by simulations in the SPICE programme.

With respect to the above discussion it can be declared that aims of this thesis were fulfilled.

6. Bibliography

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7. Appendices

7.1. Appendix A

Spice model files used for Process and electrical parameters CMOS 0.18 μ m

.MODEL CMOSN NMOS LEVEL = 7; 49

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3669193
+K1 = 0.592797	K2 = 2.518108E-3	K3 = 1E-3
+K3B = 4.7942179	W0 = 1E-7	NLX = 1.745125E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3683195	DVT1 = 0.4097438	DVT2 = 0.0552615
+U0 = 263.5112775	UA = -1.363381E-9	UB = 2.253823E-18
+UC = 4.833037E-11	VSAT = 1.017805E5	A0 = 1.9261289
+AGS = 0.4192338	B0 = -1.069507E-8	B1 = -1E-7
+KETA = -8.579587E-3	A1 = 2.789024E-4	A2 = 0.8916186
+RDSW = 126.5291844	PRWG = 0.4957859	PRWB = -0.2
+WR = 1	WINT = 0	LINT = 7.790316E-9
+XL = -4E-8	XW = 0	DWG = -1.224589E-8
+DWB = 1.579145E-8	VOFF = -0.0895222	NFACTOR = 2.5
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 2.95614E-3	ETAB = 1.374596E-4
+DSUB = 0.013974	PCLM = 0.7291486	PDIBLC1 = 0.1332365
+PDIBLC2 = 2.151668E-3	PDIBLCB = -0.1	DROUT = 0.6947618
+PSCBE1 = 7.412661E10	PSCBE2 = 1.812826E-7	PVAG = 9.540595E-3
+DELTA = 0.01	RSH = 5.9	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 8.71E-10	CGSO = 8.71E-10	CGBO = 1E-12
+CJ = 9.67972E-4	PB = 0.6966474	MJ = 0.3609772
+CJSW = 2.443898E-10	PBSW = 0.8082076	MJSW = 0.1013742
+CJSWG = 3.3E-10	PBSWG = 0.8082076	MJSWG = 0.1013742
+CF = 0	PVTH0 = 7.226579E-4	PRDSW = -4.5298309
+PK2 = -4.696208E-4	WKETA = 6.028223E-3	LKETA = -8.791311E-3
+PU0 = 17.2549887	PUA = 6.802365E-11	PUB = 4.224871E-24
+PVSAT = 1.298468E3	PETA0 = 1.003159E-4	PKETA = -3.864603E-4

*

.MODEL CMOSN NMOS LEVEL = 7; 49

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 4.1589E17	VTH0 = -0.4002789
+K1 = 0.5772615	K2 = 0.026742	K3 = 0
+K3B = 14.2532769	W0 = 1E-6	NLX = 9.883899E-8
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 0.6718731	DVT1 = 0.3118588	DVT2 = 0.1
+U0 = 118.0541064	UA = 1.626518E-9	UB = 1.229265E-21
+UC = -1E-10	VSAT = 2E5	A0 = 1.8109799
+AGS = 0.4096261	B0 = 7.705744E-7	B1 = 2.657048E-6
+KETA = 0.0212376	A1 = 0.5260122	A2 = 0.3207082
+RDSW = 306.4304418	PRWG = 0.5	PRWB = 0.0612789
+WR = 1	WINT = 0	LINT = 2.043723E-8
+XL = -4E-8	XW = 0	DWG = -4.602158E-8
+DWB = 8.005928E-9	VOFF = -0.0992452	NFACTOR = 2
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 0.0331989	ETAB = -0.0375363
+DSUB = 0.7172358	PCLM = 1.5224082	PDIBLC1 = 2.700462E-4
+PDIBLC2 = 0.0165863	PDIBLCB = -1E-3	DROUT = 1.640424E-4
+PSCBE1 = 7.71553E9	PSCBE2 = 2.228426E-9	PVAG = 5.1166248
+DELTA = 0.01	RSH = 6.7	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 6.92E-10	CGSO = 6.92E-10	CGBO = 1E-12
+CJ = 1.173089E-3	PB = 0.8524959	MJ = 0.415401
+CJSW = 2.217367E-10	PBSW = 0.5936755	MJSW = 0.2603391
+CJSWG = 4.22E-10	PBSWG = 0.5936755	MJSWG = 0.2603391
+CF = 0	PVTH0 = 1.425828E-3	PRDSW = 0.9887283
+PK2 = 1.495689E-3	WKETA = 0.0286138	LKETA = -2.746502E-3
+PU0 = -1.2891258	PUA = -5.395E-11	PUB = 1E-21
+PVSAT = -50	PETA0 = 1.003159E-4	PKETA = -2.891811E-3

*

7.2. Appendix B

Data of simulated schematics.

In this section transistor dimensions and component value and parameter are given.

Fig. 3-6. Two stages Bulk-driven OTA.

V_{DD} & $V_{SS} = \pm 0.6V$, $R = 5k\Omega$, $R_C = 4.7k\Omega$, $C_C = 0.5pF$

Transistor	Length (μm)	Width (μm)
M_1, M_2	2	30
M_3, M_4	2	4
M_5, M_8	3	20
M_6	2	16
M_7	3	40
M_9	3	10

Fig. 3-12. Bulk-driven CCII± based on Bulk-driven OTA.

V_{DD} & $V_{SS} = \pm 0.6V$, $R = 5k\Omega$, $R_C = 4.7k\Omega$, $C_C = 0.5pF$

Transistor	Length (μm)	Width (μm)
M_1, M_2	2	30
M_3, M_4	2	4
M_5, M_{16}	3	20
$M_6, M_8, M_{10}, M_{12}, M_{14}$	2	16
$M_7, M_9, M_{11}, M_{13}, M_{15}$	3	40
M_{17}	3	10

Fig. 3-19. Bulk-driven Single Input Single Output OTA (SISO) based on CCII

$V_{DD} \& V_{SS} = \pm 0.6V$, $R_{1bias} = 5k\Omega$, $R_C = 4.7k\Omega$, $C_C = 0.5pF$

Transistor	Length (μm)	Width (μm)
M_1, M_2	2	30
M_3, M_4	2	4
M_5, M_{10}	3	20
M_6, M_8	2	16
M_7, M_9	3	40
M_{11}	3	10

Fig. 3-20. Bulk-driven a fully differential OTA (DIDO) based on CCII and Voltage buffer.

$V_{DD} \& V_{SS} = \pm 0.6V$, $R_{1bias} = 5k\Omega$, $R_C = R_{C1} = 4.7k\Omega$, $C_C = C_{C1} = 0.5pF$

Transistor	Length (μm)	Width (μm)
M_1, M_2, M_{18}, M_{19}	2	30
M_3, M_4, M_{20}, M_{21}	2	4
M_5, M_{16}, M_{22}	3	20
$M_6, M_8, M_{10}, M_{12}, M_{14}, M_{23}$	2	16
$M_7, M_9, M_{11}, M_{13}, M_{15}, M_{24}$	3	40
M_{17}	3	10

Fig. 3-26. CMOS implementation of CDTA.

$V_{DD} \& V_{SS} = \pm 0.6V$, $R_{bias} = R_{1bias} = R_{2bias} = 5k\Omega$, $R_C = R_{C1} = R_{C2} = 4.7k\Omega$, $C_C = C_{C1} = C_{C2} = 0.5pF$

Transistor	Length (μm)	Width (μm)
M ₁ , M ₂ , M ₁₆ , M ₁₇ , M ₂₇ , M ₂₈	2	30
M ₃ , M ₄ , M ₁₈ , M ₁₉ , M ₂₉ , M ₃₀	2	4
M ₅ , M ₁₄ , M ₂₀ , M ₂₆ , M ₃₁ , M ₄₂	3	20
M ₆ , M ₈ , M ₁₀ , M ₁₂ , M ₂₁ , M ₂₃ , M ₃₂ , M ₃₄ , M ₃₆ , M ₃₈ , M ₄₀	2	16
M ₇ , M ₉ , M ₁₁ , M ₁₃ , M ₂₂ , M ₂₄ , M ₃₃ , M ₃₅ , M ₃₇ , M ₃₉ , M ₄₁	3	40
M ₁₅ , M ₂₅ , M ₄₃	3	10

Fig. 3-36. CMOS implementation of VDTA.

$V_{DD} \& V_{SS} = \pm 0.6V$, $R_{bias} = R_{1bias} = 5k\Omega$, $R_C = R_{C1} = R_{C2} = 4.7k\Omega$, $C_C = C_{C1} = C_{C2} = 0.5pF$

Transistor	Length (μm)	Width (μm)
M ₁ , M ₂ , M ₁₂ , M ₁₃ , M ₁₉ , M ₂₀	2	30
M ₃ , M ₄ , M ₁₄ , M ₁₅ , M ₂₁ , M ₂₂	2	4
M ₅ , M ₁₀ , M ₁₆ , M ₂₃ , M ₃₄	3	20
M ₆ , M ₈ , M ₁₇ , M ₂₄ , M ₂₆ , M ₂₈ , M ₃₀ , M ₃₂	2	16
M ₇ , M ₉ , M ₁₈ , M ₂₅ , M ₂₇ , M ₂₉ , M ₃₁ , M ₃₃	3	40
M ₁₁ , M ₃₅	3	10

Fig. 3-38. CMOS implementation of VDVTA.

V_{DD} & $V_{SS} = \pm 0.6V$, $R_{bias} = R_{1bias} = 5k\Omega$, $R_C = R_{C1} = R_{C2} = R_{C3} = 4.7k\Omega$, $C_C = C_{C1} = C_{C2} = C_{C3} = 0.5pF$

Transistor	Length (μm)	Width (μm)
$M_1, M_2, M_{12}, M_{13}, M_{19}, M_{20}, M_{36}, M_{37}$	2	30
$M_3, M_4, M_{14}, M_{15}, M_{21}, M_{22}, M_{38}, M_{39}$	2	4
$M_5, M_{10}, M_{16}, M_{23}, M_{34}, M_{40}$	3	20
$M_6, M_8, M_{17}, M_{24}, M_{26}, M_{28}, M_{30}, M_{32}, M_{41}$	2	16
$M_7, M_9, M_{18}, M_{25}, M_{27}, M_{29}, M_{31}, M_{33}, M_{42}$	3	40
M_{11}, M_{35}	3	10

Fig. 3-41. CMOS Implementation of DVCII+

V_{DD} & $V_{SS} = \pm 0.6V$, $R_{bias} = R_{1bias} = 5k\Omega$, $R_C = R_{C1} = R_{C2} = 4.7k\Omega$, $C_C = C_{C1} = C_{C2} = 0.5pF$

Transistor	Length (μm)	Width (μm)
$M_1, M_2, M_{12}, M_{13}, M_{19}, M_{20}$	2	30
$M_3, M_4, M_{14}, M_{15}, M_{21}, M_{22}$	2	4
$M_5, M_{10}, M_{16}, M_{23}, M_{28}$	3	20
$M_6, M_8, M_{17}, M_{24}, M_{26}$	2	16
$M_7, M_9, M_{18}, M_{25}, M_{27}$	3	40
M_{11}, M_{29}	3	10

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